INTERNATIONAL JOURNAL OF RESEARCH IN COMPUTER APPLICATIONS AND ROBOTICS
ISSN 2320-7345

DESIGN OF BRAUN MULTIPLIERS WITH SELF-CHECKING BASED ON TWO-RAIL ENCODING

R.Rogini[1], G.Naresh[2], K. Neelima[3]

[1]PG Student, VLSI, Sree Vidyanikethan Engineering College, Tirupati, Chittoor, A.P, India.
[2]Assistant Professor, ECE Dept., Sree Vidyanikethan Engineering College, Tirupati, Chittoor, A.P, India.
[3]Assistant Professor, ECE Dept., Sree Vidyanikethan Engineering College, Tirupati, Chittoor, A.P, India.

Abstract: - Self-checking Braun multiplier design based on two-rail encoding is an efficient method, due to its arithmetic operations and short delay. This paper presents the design of the Self-checking braun multiplier circuit can detect all single stuck-at faults during on-line operation mode. Its performance is increased by using compressor by replacing all full adders.

Keywords: Braun multiplier, full adder.

1. Introduction

A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. With advances in technology, many researchers have tried and are trying to design multipliers [5] which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. Thus making them suitable for various high speed, low power, and compact VLSI implementations. However area and speed are two conflicting constraints. So improving speed results always in larger areas. This project tries to find out the best trade off solution among the both of them. Generally multiplication goes in two basic steps. Partial product generation and accumulation.

In this project, implementation of the bypassing technique has helped in reduction of the power and area. The row bypassing is better as compared to conventional multiplier. On the implementation of column bypassing multiplier the extra circuitry needed is eliminated. The row and column bypassing multiplier results in the reduced switching activity. Thus, less power consumption.

In addition, CSeA, which is high performance, area overhead. The probability of faults, especially single-stuck-at-faults, is grown in VLSI systems. In order to guarantee highly reliability, the online detection of faults in carry select adder is important.

2. Relation between Sum Bits

Property: *The relation between sum bits calculated with identical inputs is only dependent on the carry-input, and for complemented values of carry-input, we will obtain complemented sum bits (keeping other airs of input bits identical).* [1]

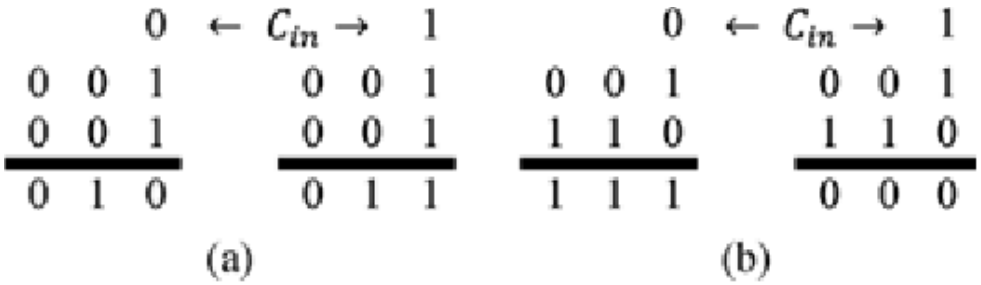


Figure.1: Examples of 3-bit addition

For the carry input cin=0,cin=1

1.For the identical inputs ,if carry input zero or one then it will be normal addition operation.

2. For the inverted inputs with carry input zero then it will be all ones.

3. For the inverted inputs with carry input one then it will be all zeros.

3. Existing System

3.1 DESIGN OF A SELF-CHECKING 2-BIT CARRY-SELECT ADDER

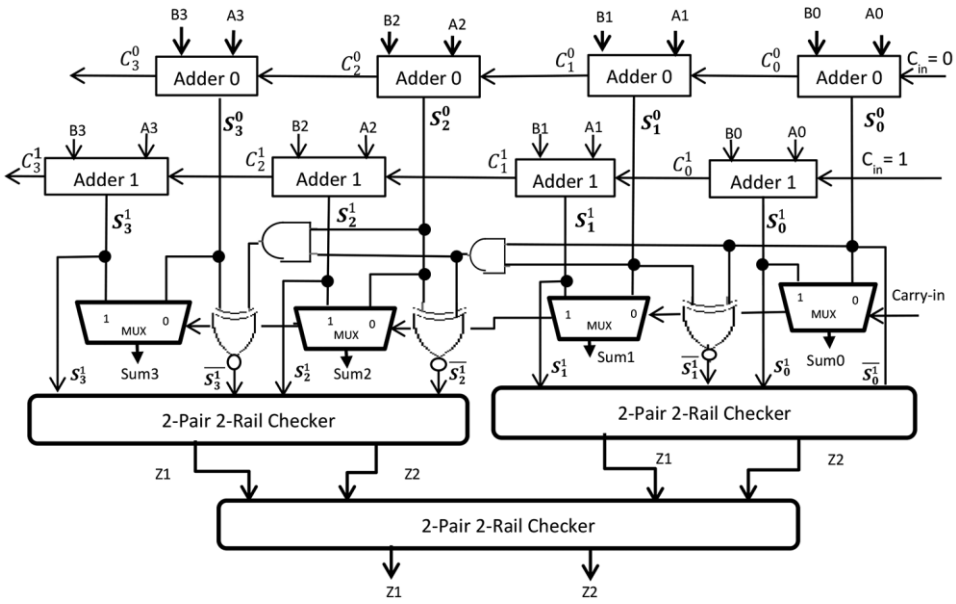


Figure.2: Existing System [1]

The stages of the self checking carry select adder design Based on two rail encoding is a chain of full adders to form ripple carry adder and it is a two rail ripple carry adders and these full adders[1] are connected to And gate and Multiplexers. The two-pair-two-rail checker has four inputs and two outputs.

3.2 Two-pair-two-rail checker

The two-pair-two-rail checker, multiplexers [2], EX-NOR can detect the presence of any single stuck-at fault in the circuit during on-line. At the primary outputs self-checking Multiplexers will detect faults internal in the circuit these faults are propagating to the output stage. At the output stage the totally self-checking checker determines the presence of the fault in the circuit.

The checker has two types i.e., 01 and 10 are considered valid code words. The inputs to the checker. A non-valid checker output, i.e., 00 or 11 detects the presence of a fault in the circuit or in the checker

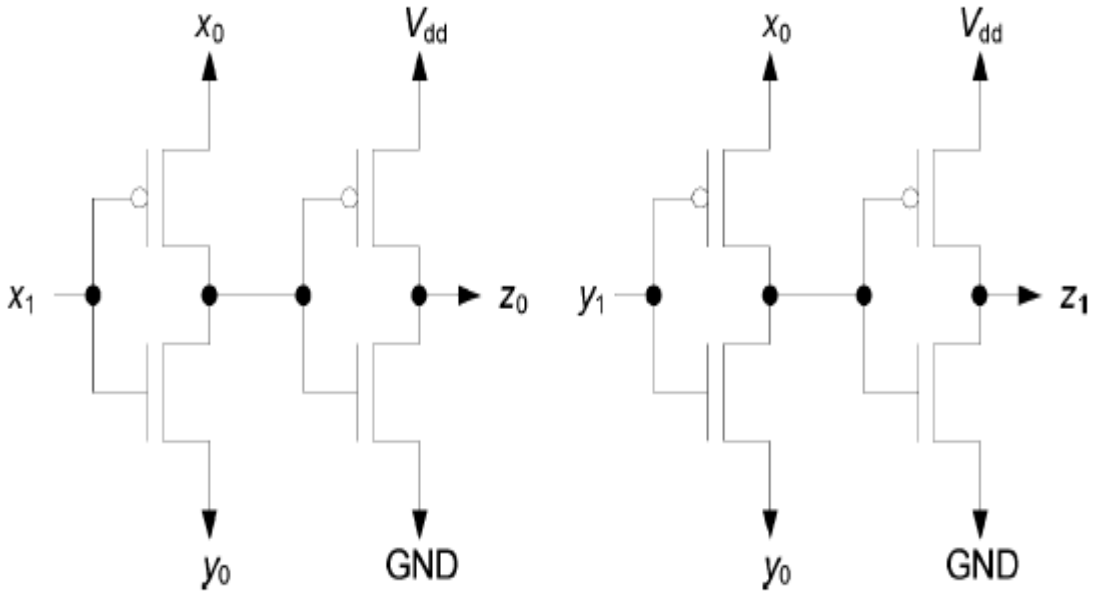


Figure.4: Two-pair two-rail checker

4. Proposed System

The proposed circuit replaces carry select adder with Braun multiplier and its architecture consists of XOR gates and multiplexers. This will increase performance of the multiplier circuit due to its self checking.

4.1 Braun Multipliers

It is a simple parallel multiplier [5] generally called as carry save array multiplier. It has been restricted to perform signed bits. The structure consists of array of AND gates and adders arranged in the iterative manner and no need of logic registers. This can be called as non –addictive multipliers. Architecture: An n*n bit Braun multiplier is constructed with n (n-1) adders and n2 AND gates as shown in the fig.1,

X: 4-bit multiplicand
Y: 4-bit multiplier
P: 8-bit product of X and Y
$P_n = X_i Y_j$ is a product bit

where, The internal structure of the full adder can be realized using FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product.

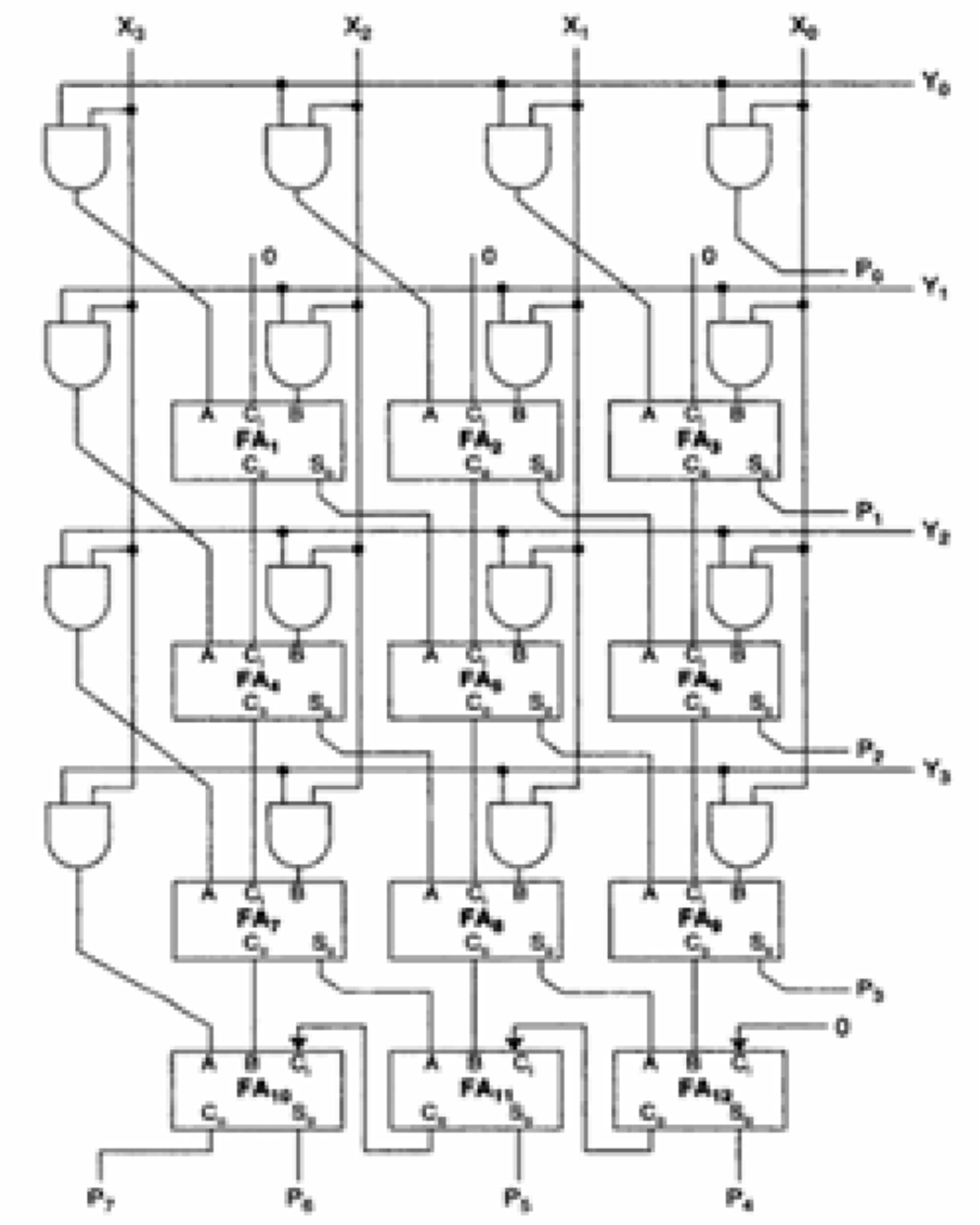


Figure.5 Braun Multiplier

The shifting would carry out with the help of Carry Save Adder (CSA) and the Ripple carry adder should be used for the final stage of the output. Braun multiplier performs well for the unsigned operands that are less than 16 bits in terms of speed, power and area. But it is simple structure when compared to the other multipliers.

5. IMPLEMENTATION

1. The proposed circuit consists of Braun multiplier, multiplexers, EX-NOR and the two-pair two rail checker Mechanism is shown in the fig

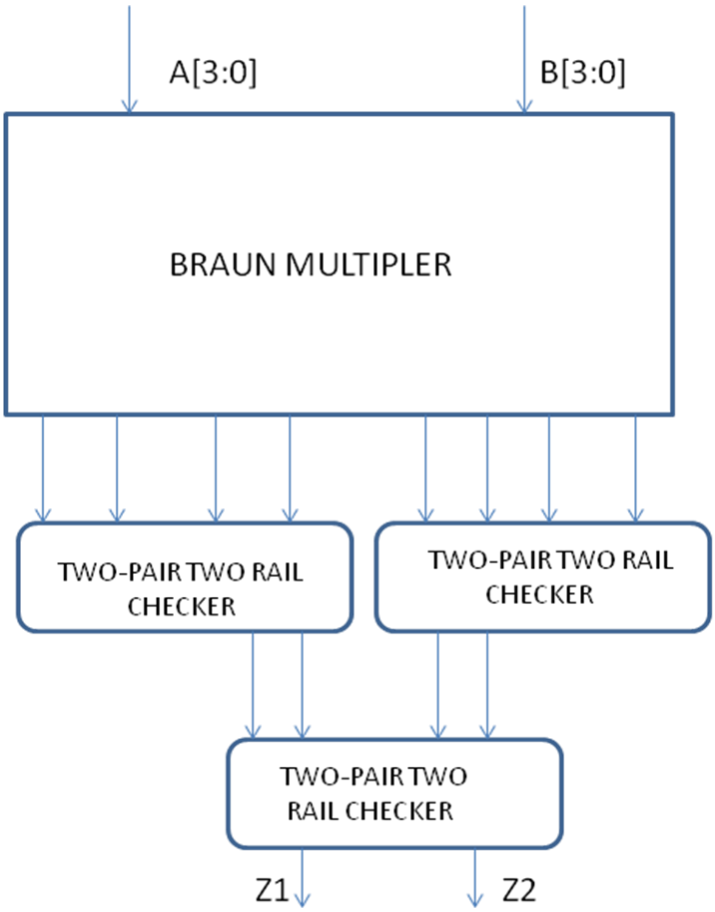
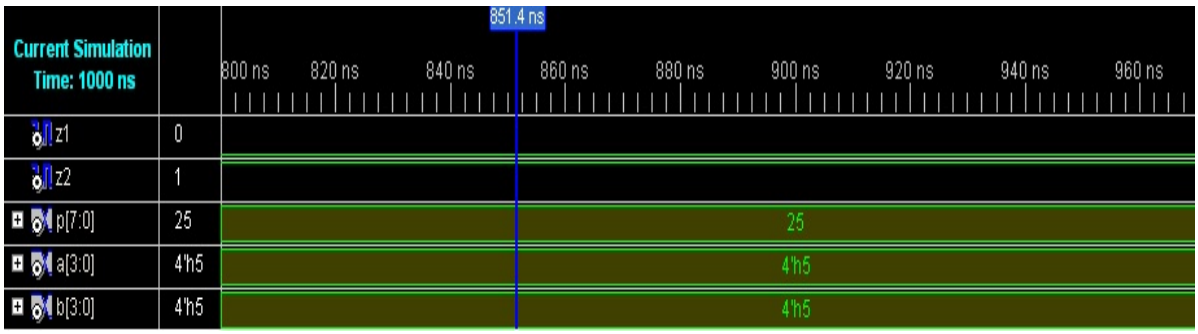


Figure 7: Proposed system

- Here it is 4-bit multiplication braun multiplier
- Braun multiplier is connected to two-pair two- rail checker in order to self-checking the multiplexer output .

6. Results And Discussion

The Proposed system is simulated and verified using Verilog HDL in Xilinx ISE 10.1.This is the simulation results for the 4 bit self Checking circuit and it is calculated for a=5,b=5.



7. CONCLUSION

This paper analyzes the self-checking Braun multiplier design based on two-rail encoding, which can be used in the testing applications purposes. In the proposed method Braun multiplier is used to overcome the limitations. Simulation results and synthesis results confirm that the proposed system has better power- delay product than existing system.

REFERENCES

[1] Muhammad Ali Akbar and Jeong-A Lee," Comments on "Self-Checking Carry-Select Adder Design Based on Two-Rail Encoding"," vol. 61, no. 7, july 2014

[2] D. P. Vasudevan, P. K. Lala, and J. P. Parkerson, "Self-checking carry select adder design based on two-rail encoding," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 12, pp. 2696–2705, Dec. 2007.

[3] Hamdi Belgacem*, Khedhiri Chiraz and Tourki Rached," A novel differential XOR-based self-checking adder"," Vol. 99, No. 9, September 2012, 1239–1261.

[4] Sanjeev Kumar and Manoj Kumar,"Low Power High Speed 3-2 Compressor" International journal of Electrical, Electronic and Mechanical controls ISSN (online): 2319-7509

[5] Anita ,Bagyaveereswaran ,"Braun's Multiplier Implementation using FPGA with Bypassing Techniques, International Journal of VLSI design & Communication Systems (VLSICS) ,"Vol.2, No.3, September 2011

R.Rogini: She is currently pursing M.Tech VLSI Sree Vidyanikethan Engineering College, Tirupati. Her areas of interest are Digital System Design, VLSI Design.

G.Naresh: He is currently working as an Assistant Professor in ECE department of Sree Vidyanikethan Engineering College, Tirupati. He has completed M.Tech in VLSI Design, in Satyabhama University. His research areas are low power VLSI Design.

K. Neelima: She is currently working as an Assistant Professor in ECE department of Sree Vidyanikethan Engineering College, Tirupati. She has completed M.Tech in VLSI Design, in Satyabhama University. Her research areas are RFIC Design, Digital Design, and VLSI Signal Processing.