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IMPLEMENTATION OF SRAM ARRAY BY USING MULTIBIT FLIP-FLOP

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Abstract: - Memory elements play a vital role on Digital World. In memory devices the most important factor is power consumption. Because the power consumption of the memory device increases means, the device reliability and life time is reduced. The basic memory elements of designer considerations are Latch and Flip-flop. In this paper we design SRAM using arrays of flip-flops and we analyze the design of Single-bit Flip-flop (SBFF i.e., 1bit) and made performance comparison over the Multi-bit Flip-flop (MBFF i.e., 2bit, 4bit, 8bit, 16bit, and 32bit). While designing the memory by using SBFF means it consumes more power. To get maximum reduction in power an algorithm has been proposed in which Single-bit flip flops are replaced with maximum possible Multi-bit Flip-flop without affecting the performance of the original circuit. This paper analyzes the timing performance of both SBFF and MBFF in Xilinx Virtex-5 family (XC5VLX50). These results in favour of Multi-Bit Flip-flop as reduction of power and area.

Keywords: Low power, Flip-flop, Latch, Merging, SBFF, MBFF, SRAM.

I. Introduction

In the past decades, the main concerns of VLSI designers were performance, area, cost and reliability. Power consumption was mostly of only secondary importance to other things. However, this has begun to change and, with major priority, power consumption is given comparable importance to area and speed. Area optimization means to optimize (reduce) the space of a digital design, such as that of an integrated circuit, while preserving the functionality [1]. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design.

Power consumption can be divided into two aspects, such as Dynamic power consumption and Static power consumption. Dynamic power is referred to as the power is consumed by a device, when it is actively switching from one state to another. Dynamic power consists of switching power, consumed while charging and discharging the loads on a device, and internal power (also referred to as short circuit power), consumed internal to the device while it is changing state. Static power is referred to as the power consumed by a device not related to state changes (also referred to as leakage power). Generally the main concern with leakage power is when the device is in its inactive state, as all the power consumed in this state is considered “wasted” power.

Designers have developed various low power management techniques to reduce power consumption, such as power gating creating multisupply voltage designs, clock gating, dynamic voltage/frequency scaling, and minimizing clock network. These techniques make use of some form of sleep operation. Placing power gating

structures is a well-known technique for reducing power leakage during standby mode, while maintaining high speeds in active mode.

II. SBFF and MBFF

In this section, we will introduce single-bit and multi-bit flip-flop conception[2]. Before that, we will review single-bit flip-flop (1-bit), it has single input is called the "DATA" input. D Flip-flop is one of the most commonly used Flip-flops. For a Positive-Edge-Triggered D Flip-flop, its output Q follows input D only at every L to H transition of CLOCK, otherwise, Q keeps unchanged. Figure 1 shows the RTL schematic of Single bit flip-flop (1-bit).

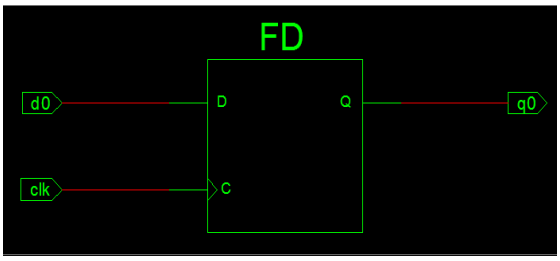

Fig. 1 RTL schematic of Single bit flip-flop (1-bit)

From the timing diagram in fig 2 it is clear that the output Q changes only at the positive edge. At each positive edge the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge.

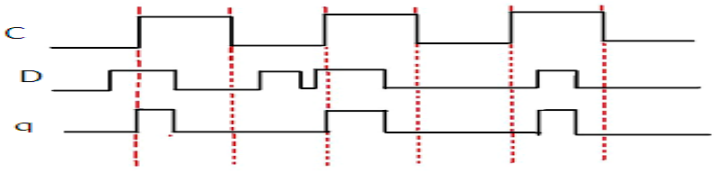

Fig. 2 Timing diagram for SBFF

The concept of merging some 1-bit flip-flops into a multi-bit flip-flop is applied to reduce dynamic clock power and decrease the total flip-flop area in a synchronous design[4]. A single-bit flip-flop has two latches (Master latch and slave latch).The latches need "Clk" and "Clk' " signal to perform operations, such as Fig. 3 shows. The multi-bit Flip-flops are mostly viewed as low power design technique, MBFFs with larger bit numbers as possible to gain more clock power saving but larger bit number may lead to severe crosstalk's due to close interconnecting wires. The single bit Flip-flop and Merging of two 1-bit flip-flops shown in the below figures.

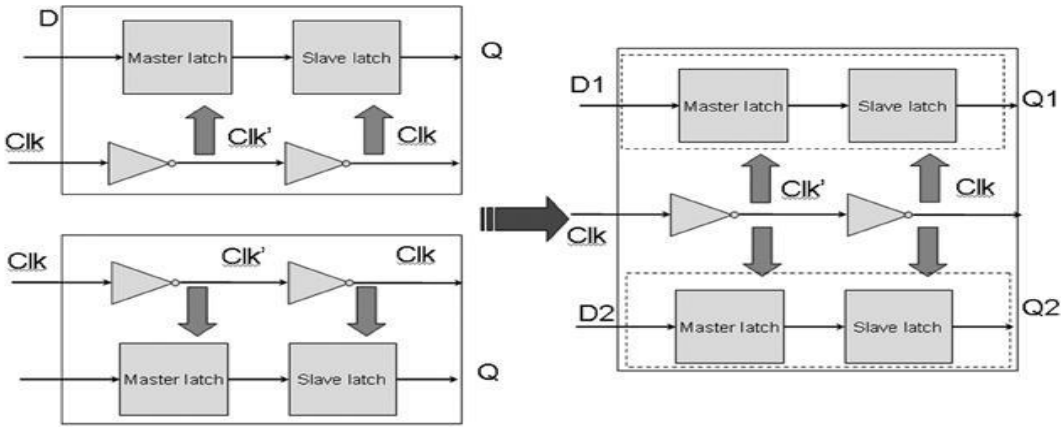

Fig. 3 merging two single bit flip-flops into one 2-bit flip-flop

Multi-bit flip-flop (2-bit, 4-bit, 16-bit, 32-bit etc....) has two or more inputs. For example consider 4-bit flip-flop, it has 4 inputs and 4 outputs shown in the below figure.

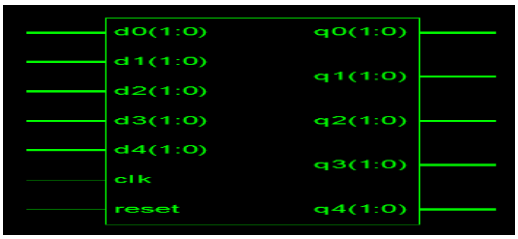

Fig. 4 RTL schematic of multi bit flip-flop (4-bit)

Multi-bit Flip-flop which takes multiple data input and results in multiple data output. The working of multi-bit Flip-flop is same as single-bit Flip-flop, whenever the clock gets active state Flip-flop latches all input to output. For inactive state the Flip-flop holds the data. The multi-bit Flip-flop corresponding waveform is given in fig 5.

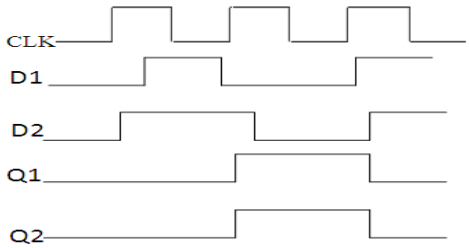

Fig. 5 Timing wave for MBFF

The MBFF has many advantages. That is

i. Area and delay is reduced.

ii. Number of inverters is reduced in clock sinks. So total power consumption is reduced.

III. SRAM

The data storage in SRAM depends on the d.c source. If the d.c is removed means, the data can be erased. SRAM means Static random-access memory, it is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. By using the Multi-Bit Flip-Flops the SRAM is designed.

SRAM 4k-bit has own input and output lines and has control signals, WRITE and PHI_b. SRAM fully operates in static mode. Therefore, no clock or refreshment is required. Testing for 4K-bit SRAM flows along the functional blocks address decoders, SRAM cell and multiplexers [3].

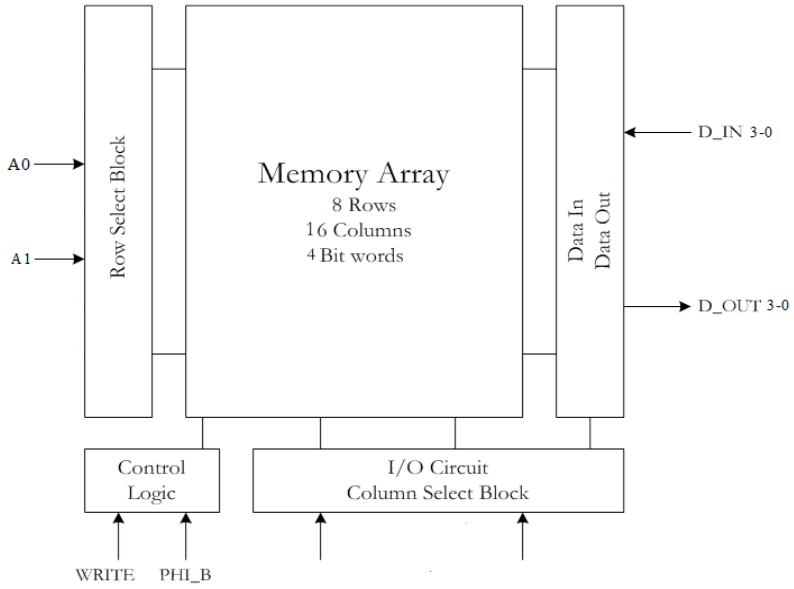

Fig. 6 4k-bit SRAM Functional block diagram

A	Address Input
D_IN	Data Input
D_OUT	Data Output
WRITE	Write Command Input
PHI_b	Bit line Pre-charge Command Input

Table I. Pin description

SRAM cell has four cases for its operation; read "1" or "0", write "1" or "0" and all of these cases were tested using Xilinx Virtex-5 family (XC5VLX50). Because SRAM cell requires a sort of tuned timing in input signals, each of PHI_b, WL, WRITE and DATAIN was set up to meet this requirement. By using address lines the flip-flop is select to write or read the data. The operation of the SRAM is, when r=0, the write operation is done. When r=1, the read operation is performed.

IV. Simulation Results

The analysis of SRAM designed using MBFF is targeted and verified on Xilinx FPGA of family Spartan-3E. The constraints taken to considerations are number of flip-flops used, clock buffer count and period analysis as Gate delay and net delay. The number of Flip-flops in SRAM using SBFF is about half a number in SRAM using MBFF. The strategies are to minimizing the power dissipation.

The Proposed system is simulated and verified using Verilog HDL in Xlinix ISE 10.1i for the target device xc3s500e-5fg320. The below simulation results show the outputs of the SBFF and MBFF.

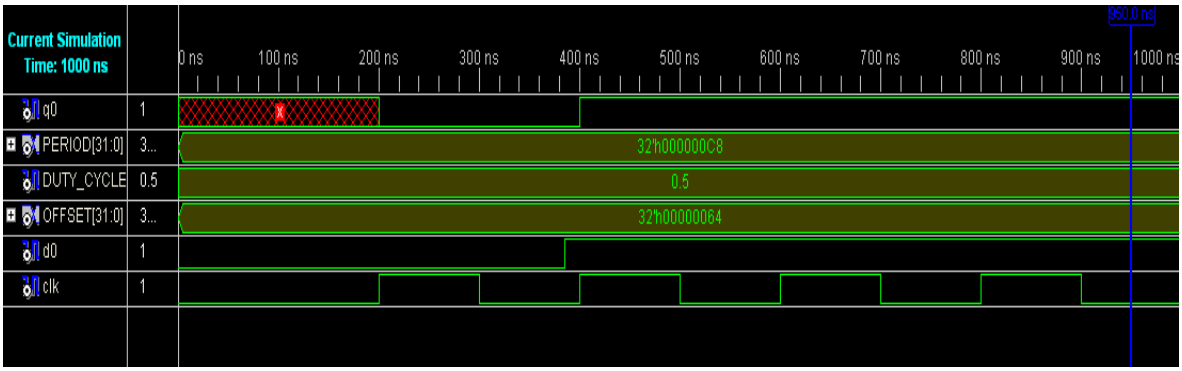

Fig. 7 Simulation result for single bit Flip-flop (1-bit)

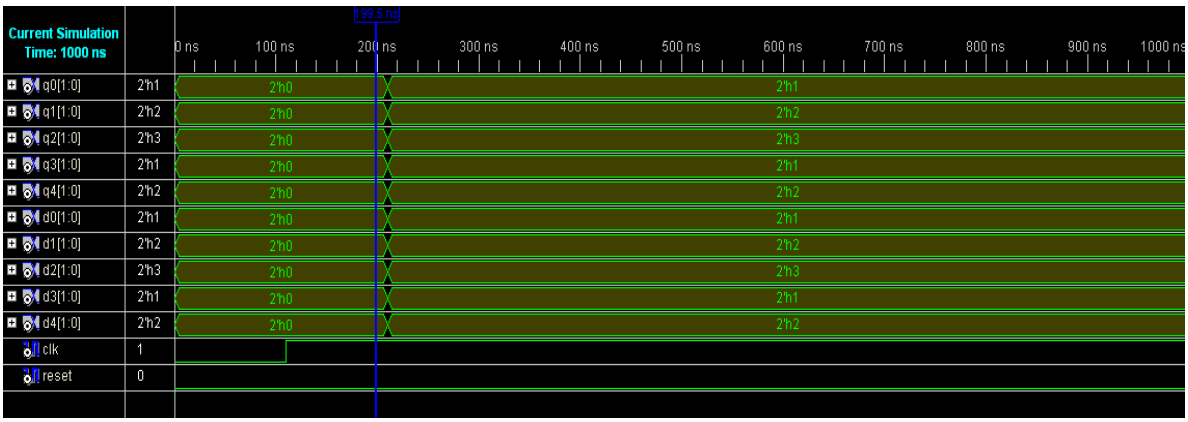

Fig. 8 Simulation result for multi bit Flip-flop (4-bit)

The synthesis result of SBFF(1-bit) and MBFF(2-bit, 4-bit, 16-bit and 32-bit) device utilization, cell usage and number of IOs shown in the below Table II, Table III and Table IV respectively.

Bit type	No. Of IOs	No. of Bonded IOBs
1-bit	3	3
2-bit	5	5
4-bit	22	20
16-bit	66	64
32-bit	130	128

Table II. Device utilization report

Bit type	IO Buffers	IBUF	OBUF
1-bit	2	1	1
2-bit	4	2	2
4-bit	20	10	10
8-bit	64	32	32
16-bit	128	64	64

Table III. Cell usage

The below Table represents the comparison of proposed method with existing method in terms of IOs

Bit type	IOs
1-bit	3
2-bit	5
4-bit	22
8-bit	66
16-bit	130

Table IV. Comparison of SBFF and MBFF IOs

V. Conclusion

In this paper, we presented Multi-Bit Flip-flops in combination with SRAM array to reduce the power consumption. The Single-Bit Flip-Flop consumes more power because of inverters in clock sinks. To reduce this power consumption MBFF is designed. In here Xilinx Virtex-5 family (XC5VLX50) tool is used to design the SRAM using MBFF. The SBFF SRAM dissipates the power as 324.16 mW and MBFF SRAM dissipates the power as 323.93 mW. So, 0.23 mW power dissipation is reduced. The Simulation Results and Power Analysis Report indicate that multi-bit flip-flop in combination with SRAM array is very effective and efficient method in lower-power designs.

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