INTERNATIONAL JOURNAL OF RESEARCH IN COMPUTER APPLICATIONS AND ROBOTICS
ISSN 2320-7345

DESIGN AND IMPLEMENTATION OF FIR FILTER USING LOW POWER BIT-SERIAL MULTIPLIER

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Abstract: - The paper proposes the implementation of low power FIR filter which is mainly based on Bit-Serial Multiplier. The proposed approach is more efficient compare to conventional FIR filter in terms of power and area. This paper presents 4x4 bit-serial multiplication technique used in signal processing and VLSI design. It's also gives the difference between canonical and transposed forms of FIR filters. Synthesis and Simulation of FIR filter is performed using Xilinx ISE 10.1i.

Keywords: Bit-serial multiplier, Parallel multiplier, FIR filter, Partial product.

1. Introduction

Nowadays many consumer electronics products and devices (e.g. Tablet) use extensive DSP techniques to implement operations such as digital filtering and image processing. FIR filter produces impulse response to any finite length input i.e., it has finite duration and settles to zero in finite time. Multipliers play major role in DSP systems and VLSI circuits. In VLSI circuit's high speed, low power and area efficient multipliers are required. Due to the trade-off between power dissipation and speed, the optimized design of multipliers is essential.

In general multipliers are classified into two types. They are bit-parallel multipliers and bit-serial multipliers. Bit-parallel multipliers process all input bits at a time in single clock cycle. Bit-parallel multipliers are generally used for high speed applications. Bit-serial multipliers process inputs serially and produces output serially. These are process a single bit of the input at every clock cycle [1]. This category of multipliers is having power and area efficient architectures, and used for low speed applications only [2-4]. These multipliers are useful in applications of bit-serial signal processing which are having and on-chip serial-link bus architectures and constrained I/O systems [5].

In this paper, we examine the efficient implementation of the FIR filter. Section II describes bit-serial multiplier which consists of bit-serial adder and partial product row generation. Section III describes 2x2 bit-serial multiplier. Section IV represents 4x4 bit-serial multiplier. Section V describes FIR filter which consumes low power and low area. Section VI gives the comparison between conventional method and proposed method in terms of area and power. Section VII represents results.

2. Bit-Serial Multiplier

Bit-serial multipliers mainly operated on FPGA's which consist of configurable logic blocks(CLBs).Each CLB consists of D flip-flop which is mainly focused by bit-serial multiplier. This multiplier generally constructed with bit-serial adder and partial product rows. Here full adder connected to D flip-flop and it produces the sum as output. It is mainly depends on the reset feature of the D flip-flop. Here full adder adds input bits x and y.

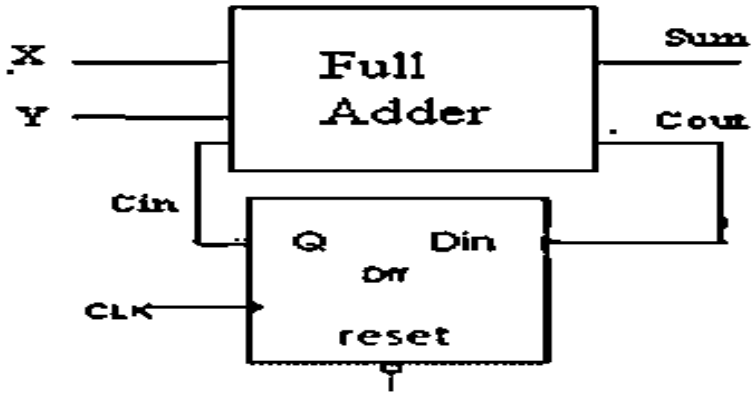

Fig.1.one bit-serial full adder

In general, partial products are generated by using AND gates. Here D flip-flop is connected to AND gate which has two inputs B_i and ctrl. Based on the reset feature of the D flip-flop it produces the pi as output.

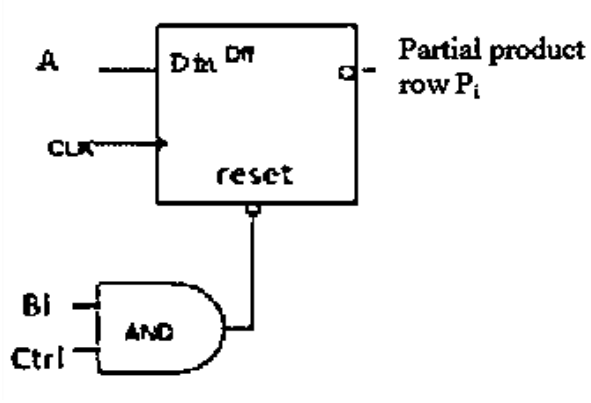

Fig.2. partial product row generation

When ctrl=0 resets DFF output Q to logic-0.For ctrl=1, when multiplier bit Bi is 0, all partial products in row are 0, not depend on the of the values of A. When B_i is 1, then Pi depend on input bits of A.

3. Design Of 2x2 Bit-Serial Multiplier

This section explains the designing of 2x2 bit-serial multiplication for inputs A and B. Here input A is applied in serial manner and input bits of B applied in parallel. This multiplication operation requires 4 clock cycles, so the the arrangement of partial product rows P0 and P1 are arranged as given below:

A_1 A_0 x B_1 B_0
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0 0 A_1B_0 A_0B_0 (Partial Product Row P_0)
0 A_1B_1 A_1B_1 0 (Partial Product Row P_1)

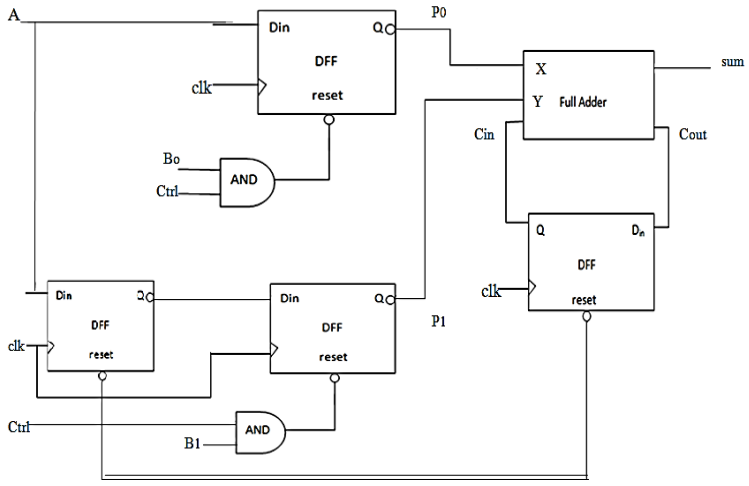

Fig.3. 2x2 bit-serial multiplier

In 2x2 bit-serial multiplier p_0 and p_1 are given as inputs to the one bit-serial full adder in order to get sum (multiplication result) as output in the above circuit.

4. Design Of 4x4 Bit-Serial Multiplier

In 4x4 bit-serial multiplication, it requires 8 clock cycles to compute the result. The required partial products rows are given below:

0 0 0 0 A_3B_0 A_2B_0 A_1B_0 A_0B_0 =>Row P_0

0 0 0 A_3B_1 A_2B_1 A_1B_1 A_0B_1 0 => Row P_1

0 0 A_3B_2 A_2B_2 A_1B_2 A_0B_2 0 0 => Row P_2

0 A_3B_3 A_2B_3 A_1B_3 A_0B_3 0 0 0 => Row P_3

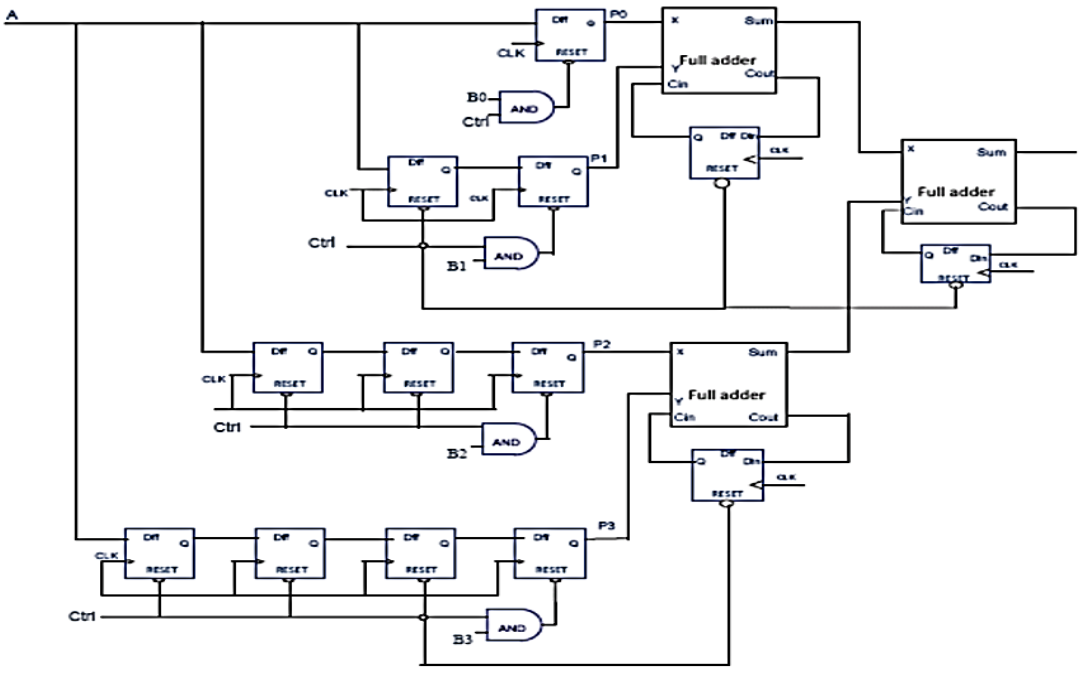

Fig.4.complete schematic diagram for 4x4 bit-serial multiplier

5. Implementation of FIR filter

Generally in signal processing systems, while processing the signal noise will be added to the applied input signal. This noise can degrade the quality of the output. To overcome this problem we have to remove the additional noise or filter out the unnecessary information. By using FIR filter we can easily remove the noise by performing the filtering operation.

FIR filters are the primary filters which are used in signal processing. FIR filter generally implemented by using a series of delays, multipliers and adders FIR filter structure can be used to implement almost any sort of frequency response digitally.

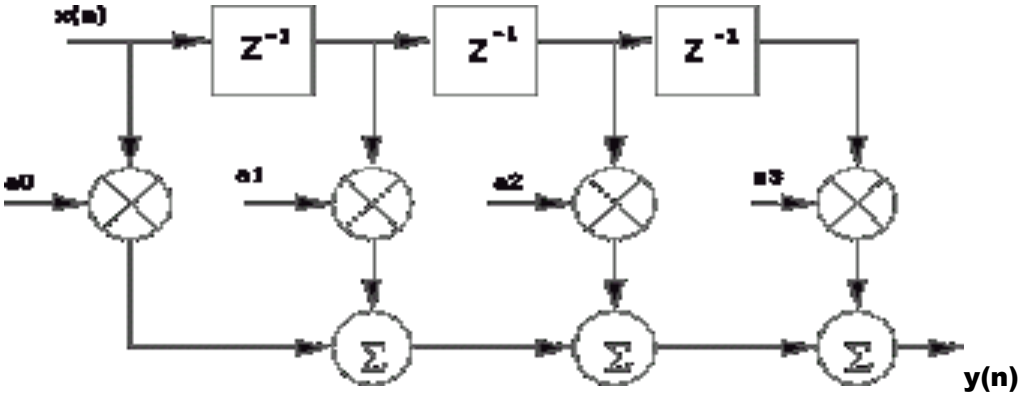

Fig.5. Block diagram of FIR filter

This FIR filter has the input x(n) and output y(n) along with the coefficients a_0,a_1,a_2 and a_3. The Nth order FIR filter having N+ 1 sample. The difference equation that gives the output of an FIR filter in terms of its input is represented as follows:

$$Y[n] = a_0 X[n] + a_1 X[n-1] + \ldots + a_N X[n-N]$$

Here instead of using general multiplier and adder we are using bit-serial multiplier and bit-serial adder in order to produce the efficient output .The input x(n) propagates serially by allowing some delays. After getting the multiplication result adding operation is performed and the final result is assigned to y(n).

6 . Simulation Results

The Proposed system is simulated and verified using Verilog HDL in Xlinix ISE 10.1i for the target device xc3s500e-5fg320. The below simulation results show the outputs of the 4x4 bit-serial multiplier and FIR filter.

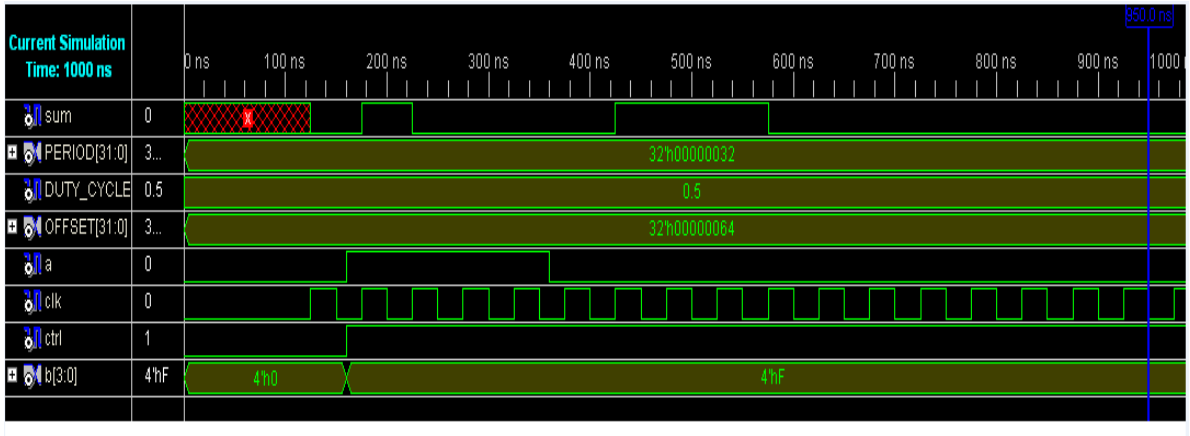

Fig.6. Simulation result for 4x4 bit-serial multiplier

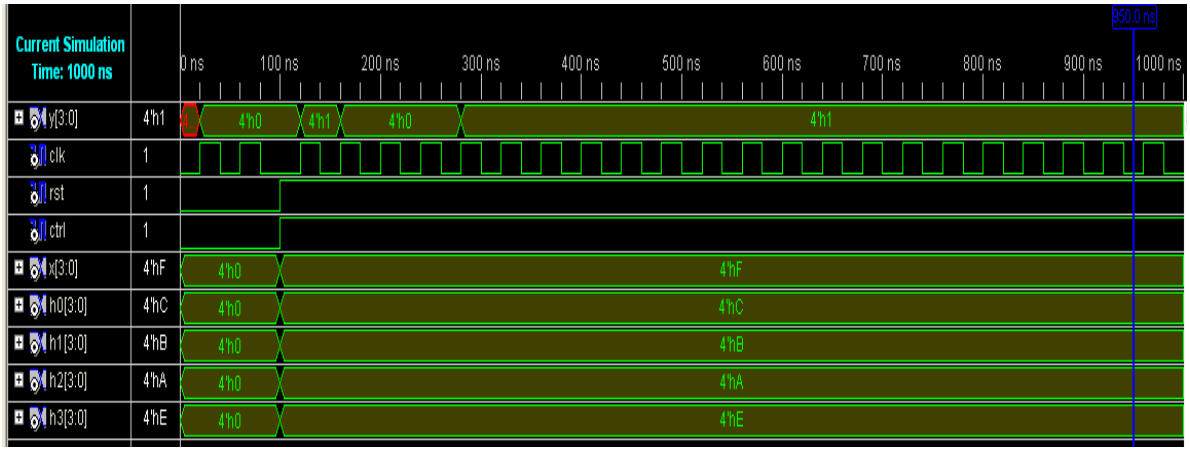

Fig.7. Simulation result for FIR filter using bit-serial multiplier

The synthesis result of 4x4 bit-serial multiplier having device utilization and timing reports with different input bits N is given in Table I and Table II respectively.

Table I. Device utilization report

N	No. Of Slices	No. of flip-flops	No. of 4 input LUTs
2	3	4	5
4	6	10	11
5	8	12	14

Table II. Timing report

N	Minimum period (ns)	Maximum frequency (MHz)
2	0.923	1083.66
4	1.456	686.74
5	1.516	659.61

The following Table represents the comparison of proposed method with existing method in terms of area, minimum period and maximum frequency.

Table. III. Comparison of general FIR filter and bit-serial multiplier based FIR filter

Parameters / Methods	Slices	LUT's	IO's	Bonded IOB's	Minimum period (ns)	Maximum frequency
General FIR filter	29	27	20	19	1.320	757.54
Fir filter with bit-serial multiplier	28	22	15	15	2.987	334.795

From the synthesis results, FIR filter with bit-seril multiplier has less area and clock frequency. In general clock frequency is directly proportional to power consumption. So power consumption is low in proposed system.

7. Conclusion

This paper analyzes the designing FIR filter with bit-serial multiplier which can be used for different applications in digital signal processing. This bit-serial multiplier mainly focused on reducing area and power. Simulation result and synthesis results confirm that the proposed FIR filter has area efficient architecture and having low power consumption.

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