INTERNATIONAL JOURNAL OF RESEARCH IN COMPUTER APPLICATIONS AND ROBOTICS
ISSN 2320-7345

IMPLEMENTATION OF ANALOG TO DIGITAL CONVERSION BY HOP FIELD NEURAL NETWORKS

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Abstract

A key component in computer based data acquisition systems is analog to digital converter (ADC). Digital communication has now become economical for widespread adoption.With the advent of high speed and high precision signal processing systems, there is a constant demand for high accuracy ADC systems. This paper investigates a novel method to implement digital conversion by Artificial Intelligence (AI) techniques in hop field networks which provide faster convergence and extremely accurate solutions for all solvable systems and ease to complexity. Counter Control ADC is used here, as it provides accurate conversion results. This approach tries to confirm data conversion is viable being both fast, reliable and economic. The mentioned work is performed using Matlab coding and simulation is also done in Labview for 4-bit ADC.

Keywords: Hop field networks, Artificial Intelligence, ADC

1. Introduction

Analog-to-digital (A/D) conversion was considered as a simple optimization problem, and an A/D converter of novel architecture was designed. A/D conversion is a simple example of a more general class of signal-decision problems which we show could also be solved by appropriately constructed networks. Circuits to solve these problems were designed using general principles which result from an understanding of the basic collective computational properties of a specific class of analog-processor networks. This approach is initially developed with reference to an ADC mathematical model, allowing the neural modelling to be properly setup. Subsequently, a neural model of a real ADC is identified and validated, highlighting the performance of the proposed approach in terms of ease of model building and result accuracy [1].

The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have been converted from a continuous time and continuous amplitude analog signal to a discrete-time and discrete-amplitude digital signal.When someone mentions the name of a

Known person we immediately recall her face and possibly many other traits. This is because we possess the so-called associative memory the ability to correlate different memories to the same fact or event. This fundamental property is not just limited to humans but it is shared by many species in the animal kingdom. Arguably the most famous example of this are experiments conducted on dogs by Pavlov [2] whereby salivation of the dog's mouth is first set by the sight of food. Then, if the sight of food is accompanied by a sound (e.g., the tone of a bell) over a certain period of time, the dog learns to associate the sound to the food, and salivation can be triggered by the sound alone, without the intervention of vision.

Since associative memory can be induced in animals and we, humans, use it extensively in our daily lives, the network of neurons in our brains must execute it very easily. It is then natural to think that such behaviour can be reproduced in artificial neural networks as well a first important step in obtaining artificial intelligence. The idea is indeed not novel and models of neural networks have been suggested over the years that could theoretically perform such function [3].

However, their experimental realization, especially in the electronic domain, has remained somewhat difficult. The reason is that an electronic circuit that simulates a neural network capable of associative memory needs two important components: neurons and synapses, namely connections between neurons. Ideally, both components should be of nanoscale dimensions and consume/dissipate little energy so that a scale up of such circuit to the number density of a typical human brain (consisting of about 10^{10} synapses/cm^2) could be feasible [4]. While one could envision an electronic version of the first component relatively easily, an electronic synapse is not so straightforward to make. The reason is that the latter needs to be flexible (”plastic”) according to the type of signal it receives, its strength has to depend on the dynamical history of the system, and it needs to store a continuous set of values (analog element). The layers of a neural network are shown in Figure 1.

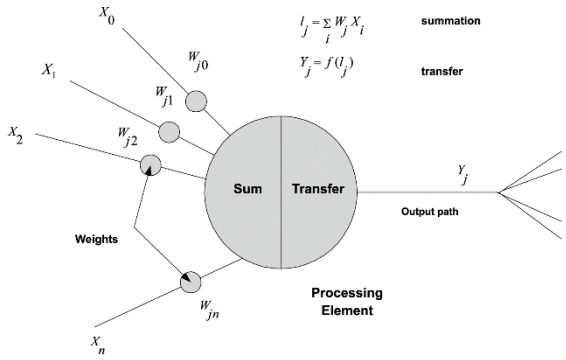

Figure 1: Layers of neural network

The building block of a neural net is the neuron. An artificial neuron works much the same way the biological one does. It takes many inputs having different weightings and has one output which depends on the inputs. A biological neuron can either 'fire' or not 'fire'(When a neuron fires, it outputs a pulse signal of a few hundred Hz). In an artificial neuron 'firing' is normally represented by a logical one and nor 'firing' by a logical zero [5].

2. Related Works

In 2000, L. N. Cooper proposed a method for Memories and memory: a physicist's approach to the brain [1]. In 2007, Deepak Mishra and Prem K. Kalra proposed modified Hopfield neural network approach for solving nonlinear algebraic equations [2]. In 2010, Yuriy V. Pershin and Massimiliano Di Ventra proposed an experimental demonstration of associative memory with memristive neural networks [3]. In 2011, Hardware Implementation of an ADC compensation using neural networks was done by HerveChanal [4]. In 2008, T. Munakata, demonstrated Fundamentals of the New Artificial Intelligence: Neural, Evolutionary, and Fuzzy [5].

3. Hop Field Network

A Hopfield network is a form of recurrentartificial neural network invented by John Hopfield in 1982. Hopfield nets serve as content addressable memory systems with binary threshold nodes. They are guaranteed to converge to a local minimum, but convergence to a false pattern (wrong local minimum) rather than the stored pattern (expected local minimum) can occur. Hopfield networks also provide a model for understanding human memory [6].The units in Hopfield nets are binary threshold units, i.e. the units only take on two different values for their states and the value is determined by whether or not the units' input exceeds their threshold. Hopfield nets normally have units that take on values of 1 or -1. Every pair of units i and j in a Hopfield network have a connection that is described by the connectivity weight w_{ij}. In this sense, the Hopfield network can be formally described as a complete undirected graph

G = < V,f >,

Where V is a set of McCulloch-Pitts neurons and f : V2 -> R is a function that links pairs of nodes to a real value, the connectivity weight.

The connections in a Hopfield net typically have the following restrictions:

Wii = 0 (no unit has a connection with itself)

Wij = wjiconnections are symmetric)

The requirement that weights be symmetric is typically used, as it will guarantee that the energy function decreases monotonically while following the activation rules, and the network may exhibit some periodic or chaotic behaviour if non-symmetric weights are used. However, Hopfield found that this chaotic behaviour is confined to relatively small parts of the phase space, and does not impair the network's ability to act as a content-addressable associative memory system. A Hopfield with 6 nodes is shown in Figure 2.

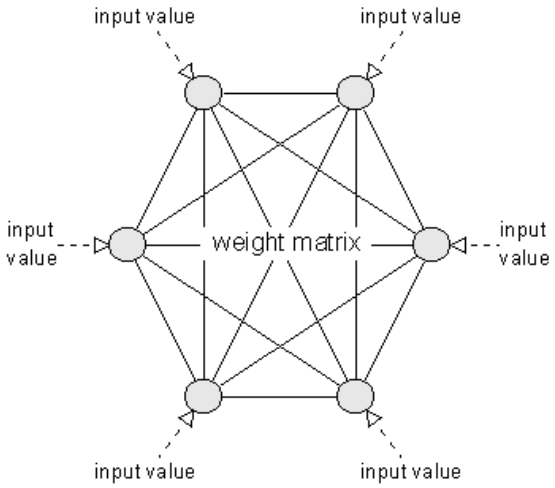

Figure 2: A Hopfield net

4. Digital Conversion by Hop Field

Counter Control ADC is shown in Figure 3. The N bit counter generates an n bit digital output which is applied as an input to the DAC. The analog output corresponding to the digital input from DAC is compared with the input analog voltage using an opamp comparator. The opamp compares the two voltages and if the generated

DAC voltage is less, it generates a high pulse to the N bit counter as a clock pulse to increment the counter. The same process will be repeated until the DAC output equals to the input analog voltage.

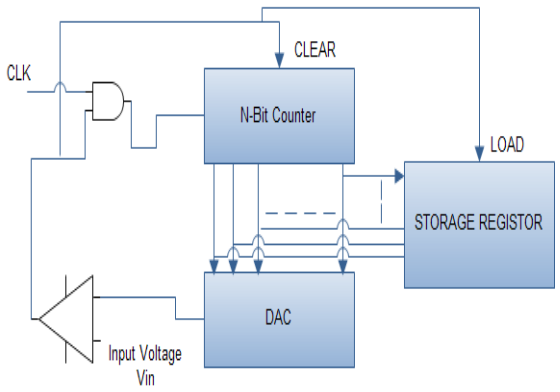

Figure 3: Counter type ADC

If the DAC output voltage is equal to the input analog voltage, then it generates low clock pulse and it also generates a clear signal to the counter and load signal to the storage resistor to store the corresponding digital bits. These digital values are closely matched with the input analog values with small quantization error. Hopfield type architecture for solving the nonlinear equation is shown in Figure 4.

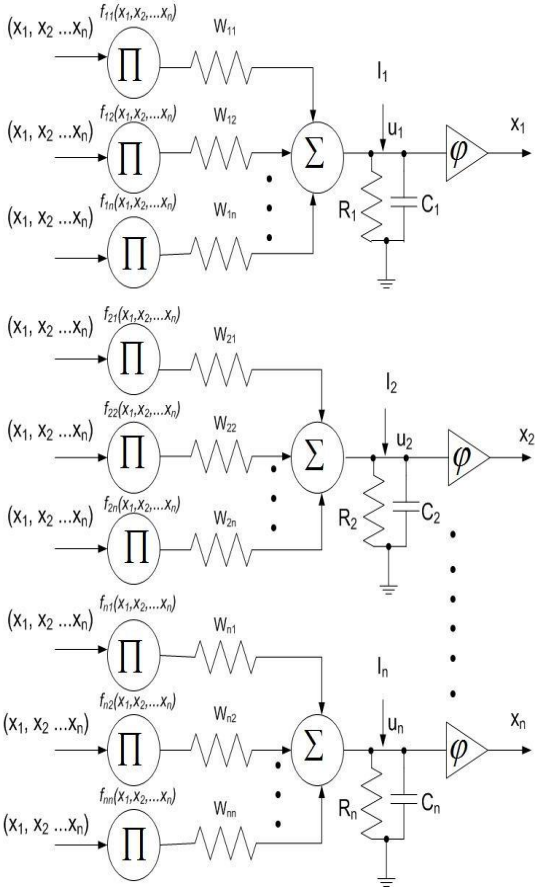

Figure 4: Hopfield type architecture for solving the nonlinear equation

5. Implementation Results

Using MATLAB R2010a, noisy analog signals and their equivalent digital representations were generated.Here we add some Gaussian noise to the input sine wave and then the signal is converted to digital signal. The analog-to digital converter simulated using hop field in neural network is shown in Figure 5.

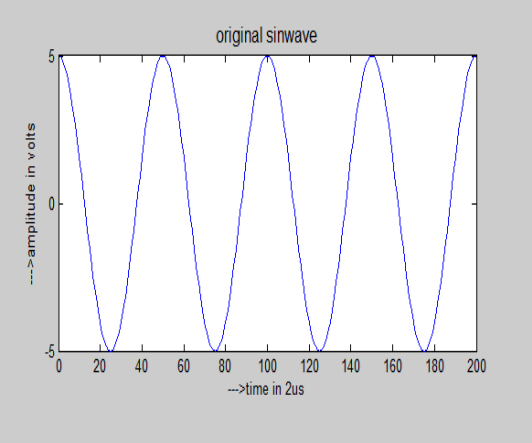

Figure 5a): Input signal

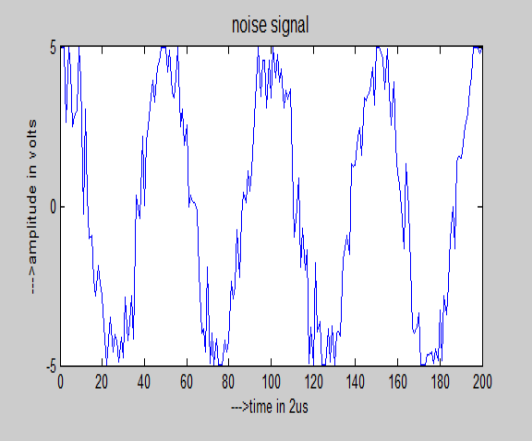

Figure 5b): Gaussian Noise Signal

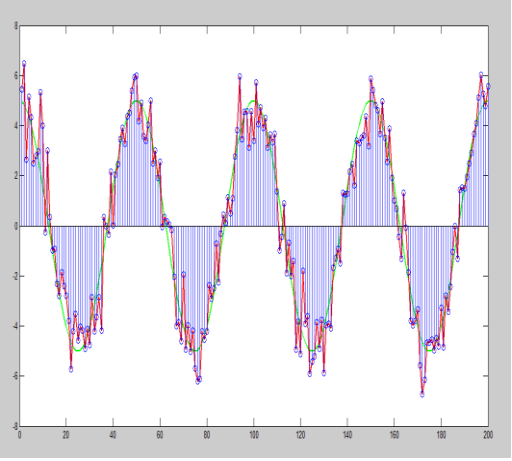

Figure 5c): Simulated Analog-to-Digital conversion in MATLAB

Simulation is performed for a 4 bit ADC in Lab View for an analog input of 50V and the array represents the amplitude of the sampled signals. The input analog and the output digital signal are represented in Figure 6.

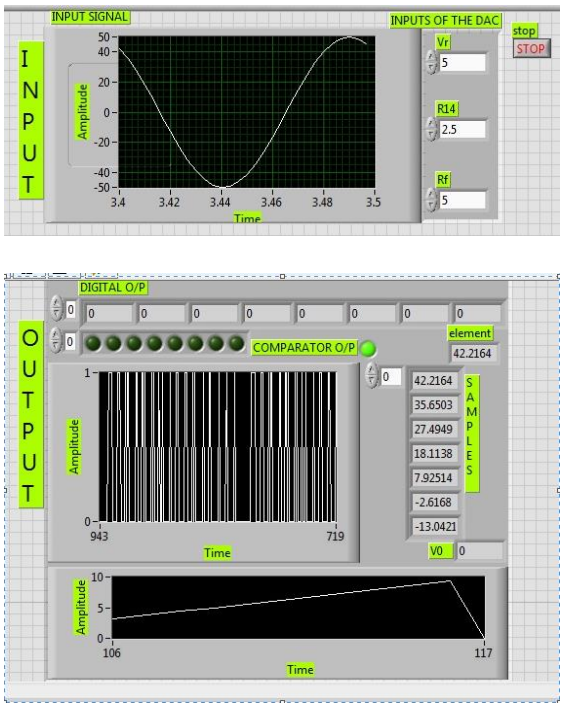

Figure 6: Labview output for Analog signal with 50V input

6. Conclusion

This paper thus shows implementation of a high precision high accuracy ADC approaches for A to D conversion by Artificial Intelligence (AI) techniques in hop field networks.Thus a neural model of a counter control ADC is identified and validated, highlighting the performance of the proposed approach in terms of ease of model building and result accuracy. This approach thus confirms data conversion is viable being both fast, reliable and economic.

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