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GROUND BOUNCE NOISE REDUCTION USING HIGH SPEED AND LOW POWER 14T FULL ADDER

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Abstract

In low power design circuits the leakage power and ground bounce noise are plays a virtual role in the any module. The leakage power consumption and ground bounce noise are effects a performance of the module. In digital electronics adders are used to addition operation. Adders are used in many applications and adders are not only performing the arithmetic operation but adders also used to generate the address in processors and many controllers. In this paper we are designing the low power 14Transistor full adder for the purpose of reducing ground bounce noise in mobile applications. Here we are designing the 14T full adder using 7 NMOS and PMOS Transistors. Using Digital schematic (DSCH) software we are designing the 14Transistor full adder and simulation result is performed by the microwind3.1 software.

Keywords: Low power, Adders, Ground bounce noise, DSCH, Micro wind, Transistor.

1. Introduction

In digital electronics, the adders play a virtual role in computational circuits like compressors, multipliers, comparators and parity checkers. In today's world, implementation of low power full adder has been proposed using different logics. The main aim of the project is we are implementing the 14T full adder to reduce the noise and increase the speed. The designed 14T full adder main aim is improvement of power efficiency and ground bounce reduction using 45nm technology. In digital electronics, ground bounce Noise is a sensation affiliate with transistors switching. In the transistor switching the gate voltage will be less than the local ground voltage. Here we are designing the 14T full adder using seven NMOS and PMOS transistors. The low power 14T full adder reduces the ground bounce noise and its working with the high performance. In any logic circuit the power reduction is mainly based on the tradeoffs between the transistors. In this paper we are proposing the different techniques to reduce the power and increase the performance. Mainly the ground bounce noise is occurred in high consistency Very large scale integration where deficient precautions have been appropriated to inventory a logic gate with abundantly connect low resistance to ground.

2. Full adder

The adder plays a key role in digital electronics. Here we have the basic adders like half adder and full adder. The adders not only performing the arithmetic operations it's also used to perform the different operations in microprocessors, controllers and DSP applications. Using two half adders we are designing the full adder. Full adder is nothing but it is the addition of three binary digits. Full adder has the three inputs A, B, C in and two outputs sum and carry. Using these basic adders we are designing the different adders like Ripple carry adder, Carry select adder, Carry Look ahead adder and Carry Save adder. Mainly in many processors and controllers are used to increase the performance of the module.

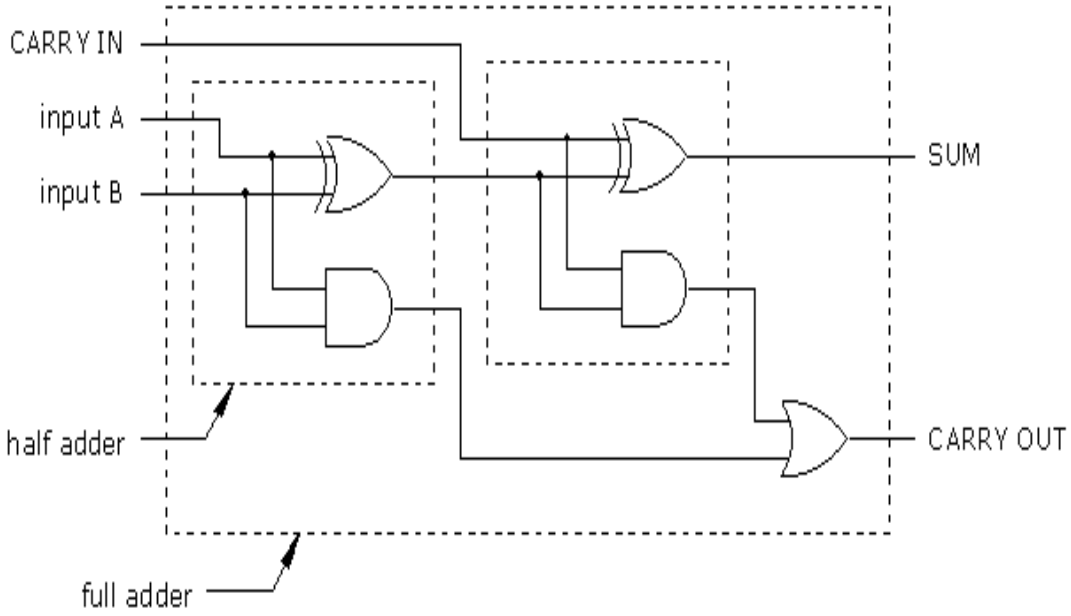

Fig1: Full adder design using two half adders

3. Low Power 14T Full adder

Here we are designing the low power 14T full adder using seven NMOS and PMOS transistors. The transistor acts as a switch and Transistor here we have NMOS and PMOS transistors. The PMOS transistor configuration is reverse to the NMOS configuration. When NMOS will be ON the PMOS will be in OFF condition as well as when NMOS will be OFF the PMOS will be ON. Here the NMOS and PMOS transistors are working with low power and high speed.

The 14T full adders have the less number of transistors for the reduction of low leakage power; here the 14T Full adder suffers with the ground bounce Noise. In this paper we are proposing the 14T full adder without sleep Transistor and another one is 14T full adder with Sleep Transistor. To reduce the Ground Bounce Noise in mobile applications we are using the sleep transistor. When the total Design will be ON the sleep transistor will be in the OFF condition at that time the ground voltage is equal to zero and power supply will be high so automatically Ground Bounce Noise will be reduced by the design. Without sleep transistor 14T full adder and with sleep Transistor 14T full adder is shown in below figures.

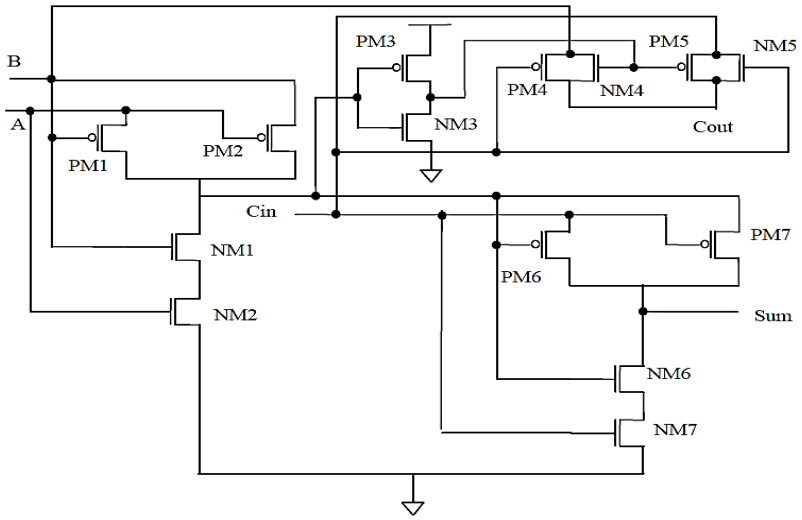

Fig2: 14T Full adder without sleep Transistors

Here with the help of selected switch (sleep transistor switch) we are reducing the Ground bounce Noise in mobile applications and it is achieved by the adjusting the both sleep transistors1 and 2 with the help of delay time(delay between the two sleep transistors).

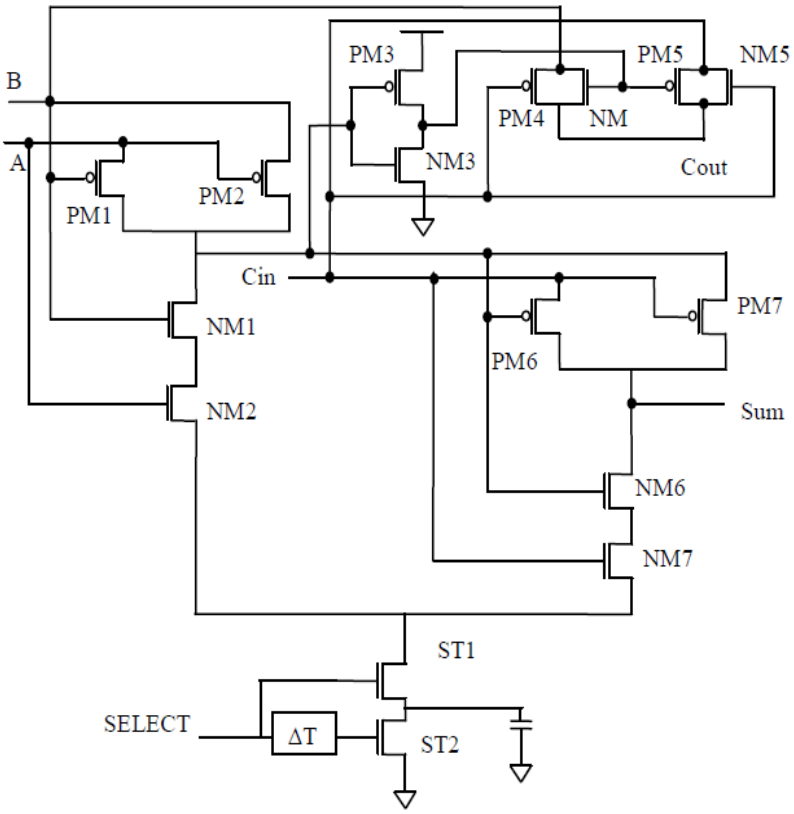

Fig3: 14T full adder with sleep Transistor

4. Simulation Results

The 14T full adder without sleep transistor and 14T full adder with sleep transistor is designed in Digital Schematic (DSCH) software. In this software we are designing the design and we are generating the verilog file. This verilog file will be in the form of .V and this file will be compiled in the microwind tool. When we are compiling the .V file in microwind tool automatically we are getting the layout diagram and simulation results. The 14T full adder satisfies the three basic things in VLSI those are SPEED, AREA, and POWER.

Fig4: simulation result of 14T full adder

5. Conclusion

To reduce the ground bounce noise and leakage power we are implementing the 14T full adder using seven NMOS and PMOS transistors. These 14T full adder design is working with the low power to reduce the ground bounce noise we are using the sleep Transistor. Here we use high speed power gating technique to reduce the leakage power and ground bounce noise in mobile applications. The modified 14T full adder with sleep transistor is works with the various voltages levels.

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