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EFFICIENT APPROACH TO OPTIMIZE QUANTUM COST FOR COMBINATIONAL REVERSIBLE CIRCUITS

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Abstract—Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of reversible computation. This has led to the development of reversible gates. This Paper introduces new synthesis approach called Exorlink which reduces quantum cost compared to the technique Disjoint Sum of Products (DSOP) when used in the design of reversible circuits. The design is coded in VHDL, simulated using ISIM and synthesized using Xilinx ISE 10.1i for the device Spartan3E FPGA.

Index Terms—Reversible Circuits, Disjoint Sum of Products (DSOP), Exorlink, Quantum Cost.

INTRODUCTION

Energy dissipation is one of the major issues in present day technology. Improvement in technology leads to compactness in size of system and increase in execution speed. Due to this energy dissipation is increased by the system. It can be explained from Moore's Law that over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every two years. The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper. His prediction has proven to be accurate, in part because the law is now used in the semiconductor industry to guide long-term planning and to set targets for research and development. The capabilities of many digital electronic devices are strongly linked to Moore's law: processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras. All of these are improving at roughly exponential rates as well. This exponential improvement has dramatically enhanced the impact of digital electronics in nearly every segment of the world economy.

Moore's law describes a driving force of technological and social change in the late 20th and early 21st centuries. The period is often quoted as 18 months because of Intel executive David House, who predicted that chip performance would double every 18 months (being a combination of the effect of more transistors and their being faster)[2].

Although this trend has continued for more than half a century, Moore's law should be considered an observation or conjecture and not a physical or natural law. Sources in 2005 expected it to continue until at least 2015 or 2020. However, the 2010 update to the International Technology Roadmap for Semiconductors predicted that growth will slow at the end of 2013, when transistor counts and densities are to double only every

three years[1]. In 1961, Rolf Landauer in his principle stated that the heat coming from computation was due to the destruction of information (wiping out bits of information) and not to the processing of bits.

Landauer showed that for every bit of information that is erased during an irreversible logic computation KTln2 joules of heat energy is generated, where K is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components [2].

In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials [3][4]. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss over the last decades. The power dissipation in a circuit can be reduced by the use of Reversible logic.

Bennett showed that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. Several such gates are proposed over the past decades.

A reversible logic circuit should have the features like usage of minimum number of reversible gates, garbage outputs and constant inputs. Among these minimization of the garbage outputs is one of the major goals in reversible logic design and synthesis. Reversible Logic is becoming more and more prominent technology having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing.

Each Reversible gate has a cost associated with it called Quantum Cost. The Quantum Cost of a circuit is defined by the total number of elementary quantum gates needed to realize the given function. Quantum Cost of a circuit is proportional to the heat dissipation in the circuit. For any function realized using various types of gates, the Quantum Cost is given by the sum of the Quantum Costs of all the gates used to realize that function.

In section II the existing method of computing quantum cost by DSOP method is discussed. Section III deals with the proposed method Exorlink for evaluating the quantum cost. In section IV the results are discussed and compared. Section V concludes the paper.

II PSOP METHOD

The basic differences between the various definitions are given below.

A Boolean expression is an algebraic clause representing a relationship among a set of Boolean valued literals [4]. A Boolean function can be represented by an equation containing Boolean expressions.

F=x’·y’·z’+z ---------- (1)

A Boolean expression containing a set of literals conjuncted together (i.e. ANDed) is called a Product/Cube.

F=x’·y’·z’ ---------- (2)

The inclusive OR function in Boolean algebra is called Disjunctive Sum.

F=x’ + z ---------- (3)

Two or more AND functions are ORed together to form a Sum-of-products expression. In this form, the product terms may or may not cover a common minterm.

F=w·y’+x+y·z ---------- (4)

Two cubes are said to be disjoint if their intersection of the set of minterms is null i.e., Disjoint cubes.

F(w,x,y,z)=w'x and G(w,x,y,z)=x'z ---------- (5)

The distance of two min terms is the number of variables for which the corresponding literals have different sets of values.

i.e., the distance between 1011 and 0111 is 2

A cube cover corresponds to the familiar sum-of-products representation in Boolean Algebra with each cube corresponding to a product term and the function being the sum (logical OR) of those terms. Since a single cube represents a Boolean function on its own, the set of cubes
representing a Boolean function not necessarily be unique[5]. A case of interest is when each pair of cubes in the cover is disjoint, that is, when the two cubes do not share a common
minterm. Such a situation corresponds to a Disjoint Sum-of-Products (DSOP) expression.

The example for conversion of SOP Expression to DSOP Expression is as shown in Fig.1.

Let the Sum of Product Expression be

F=abc'+bc'd+abc'd+a'bcd+ab'c+acd' ---------- (6)

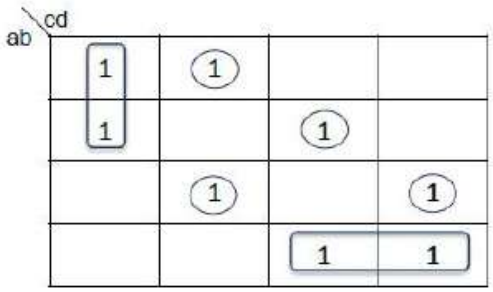


Fig.1: DSOP K-map for eq.6

Then the Disjoint Sum of Product Expression from fig.1 is given by eq.7.

F=a'c'd' ⊕ a'b'c'd ⊕ abc'd ⊕ a'bcd ⊕ abcd' ⊕ ab'c -- (7)

Hence if no two product terms cover a common minterm, they are called a disjoint-sum-ofproducts (DSOP).

III EXORLINK METHOD

For Exorlink Operation between two terms is as shown below

1. Replace the bit changed with 'x' or '0' or '1' depending on the bits in the two terms [6].
2. The left side of the changed bit is replaced with the bits in the first term.
3. The right side of the changed bit is replaced with the bits in the second term.

Eg.: $1011 \otimes 0111 = x111 \oplus 1x11$

$x0x1 \otimes 1001 = 0001 \oplus x011$

The Reversible Circuit's DSOP and Exorlink equations and their Quantum Cost is given below.

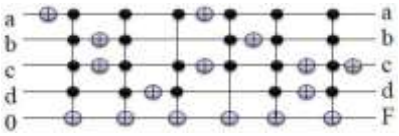


Fig.2: Reversible circuit for DSOP

The DSOP Expression is given by

F=a'c'd'⊕a'b'c'd⊕abc'd⊕a'bcd⊕abcd'⊕ab'c ---- (8)

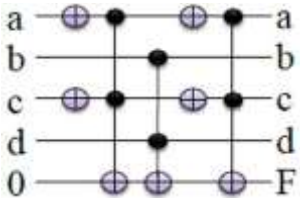


Fig.3: Reversible Logic for Exorlink

The Exor Expression is given by

F= a'c'⊕bd⊕ac ---- (9)

Algorithm for conversion of DSOP to Exorlink

1. Convert the terms in DSOP equation into binary form.
2. Find the distance between all possible pair of terms.
3. Select a pair of terms having minimum distance (1 or 2 or 3) if exist.
4. Choose the order of the terms to perform exorlink operation such that the resultant terms will have minimum distance with the other terms.
5. Perform Exorlink operation and replace the xorlinked terms with resultant terms and if any pair have distance 1, perform exorlink operation on the pair.
6. If not check for links in k-map.
7. a) If links are not formed between all the pairs, repeat from step 2.

   b) If links are formed between all pairs, write the corresponding exorlink equation.

Fig.4: Algorithm for Conversion of reversible circuit from DSOP to Exorlink

IV RESULTS AND DISCUSSION

A Full Adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and three outputs[8]. Two of the input variables denoted by A and B, represent the two significant bits to be added. The third input, represents the carry from the previous lower significant position.

The truth table of full adder circuit is as shown in Table.1

Table.1: Truth Table for Full adder

Inputs			Outputs	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

SOP form: Sum: S = A ⊕□B ⊕C
Carry: Cout = AB + AC + BC
DSOP: S = AB'C' ⊕□A'B'C ⊕□ABC ⊕□A'BC'

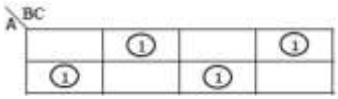


Fig.5: K-map for SUM

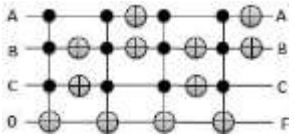


Fig.6: DSOP Reversible Circuit for SUM

Quantum Cost: 4 * 13 + 8 = 60

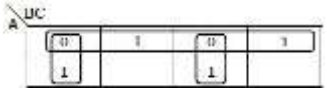


Fig.7: Exorlink K-MAP for SUM

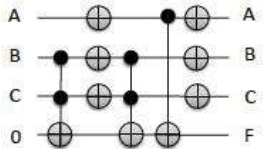


Fig.8: Exorlink Reversible Circuit for SUM

Exorlink: S = A' ⊕ B'C' ⊕ BC
Quantum Cost: 2*5 + 7 = 17

DSOP: Cout = AB ⊕ A'BC ⊕ AB'C

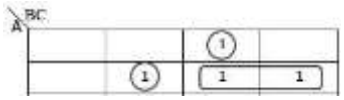


Fig.9: K-Map for carry

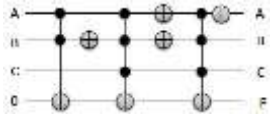


Fig.10: DSOP Reversible Circuit for Carry

Quantum Cost: 2*13 + 5 + 4 = 35
Cout = AB ⊕ BC ⊕AC

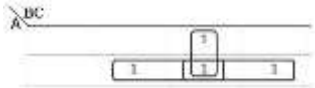


Fig.11: Exorlink K-map for carry

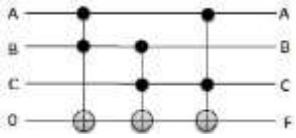


Fig.12: Exorlink Reversible Circuit for Carry

Quantum Cost: 3*5 = 15

Table.2: Total Quantum Cost for Full Adder

Full Adder	Total Quantum Cost
DSOP Reversible Circuit	60+35=95
Exorlink Reversible Circuit	17+15=32

A Full Subtractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. Three input are A, B, and C, denote the minued, subtrahend, and previous borrow, respectively [9]. The two outputs D and B0 represent the difference and output borrows, respectively.

Table.3: Truth Table for Full Subtractor

Inputs			Outputs	
A	B	C	D	BO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

SOP:
Difference = A'B'C + A'BC' + AB'C' +ABC
Borrow = A'C + A'B + BC
Difference:
DSOP:D=AB'C'⊕ A'B'C⊕ ABC⊕ A'BC'

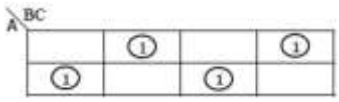
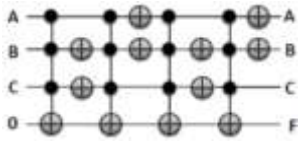


Fig.13: K-map for Difference Fig.



14: DSOP Reversible Circuit for Difference

Quantum Cost = 4*13 + 8 = 60
Exorlink:D=A'⊕ B'C'⊕ BC

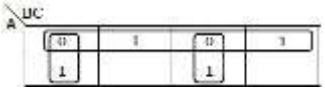


Fig.15: Exorlink K-MAP for SUM

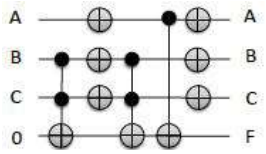


Fig.16: Exorlink Reversible Circuit for SUM

Quantum Cost: 2*5 + 7 = 17
Borrow:
DSOP : B0 = A'B ⊕ A'B'C ⊕ ABC

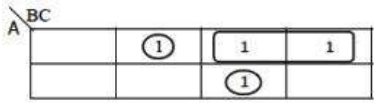


Fig.17: K-Map for Borrow

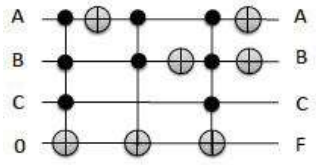


Fig.18: DSOP Reversible Circuit for Borrow

Quantum Cost = 2*13 + 5 + 4 = 35
Exorlink:B0=A'C⊕A'B⊕ BC

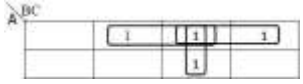


Fig.19: Exorlink K-map for Borrow

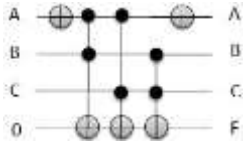


Fig.20: Exorlink Reversible Circuit for Borrow

Quantum Cost = 3*5 + 2 = 17

Table.4: Total Quantum Cost for Full Subtractor

Full Subtractor	Total Quantum Cost
DSOP Reversible Circuit	60+35=95
Exorlink Reversible Circuit	17+17=34

Comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes[8]. The outcome of comparison is specified by three binary variables that indicate whether **A>B, A=B, or A<B.**
The truth table of Comparator circuit is as shown in Table.3.

Table.5: Truth Table of Comparator Circuit

A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

A>B:
DSOP:F=A1A0B1B0'⊕A1'A0B1'B0'⊕A1B1'

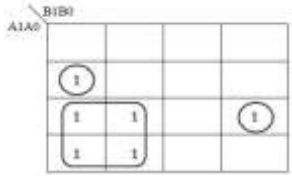


Fig.21: DSOP k-map for A>B

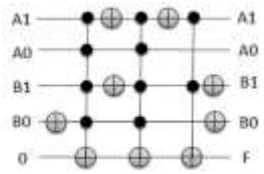


fig.22: DSOP Reversible Circuit for A>B

Quantum Cost: 2*29 + 6 +5 = 69
Exorlink:F=A1A0B0'⊕A0B1'B0'⊕A1B1'

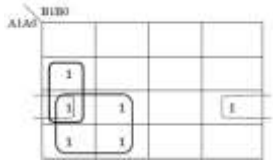


Fig.23: Exorlink k-map for A>B

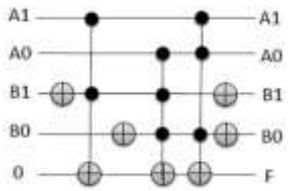


fig.24: Exorlink Reversible Circuit for A>B

Quantum Cost: 2*13 + 5 + 4 = 35
A=B:
DSOP: F=A1'A0'B1'B0'⊕A1'A0B1'B0⊕A1A0B1B0⊕A1A0'B1B0'

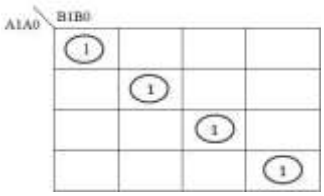


Fig.25: DSOP k-map for A=B

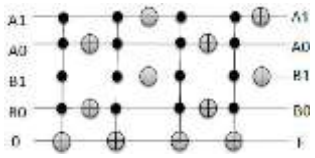


fig.26: DSOP Reversible Circuit for A=B

Quantum Cost: 4*29 + 8 = 124

Exorlink:F=B1B0⊕A1'B0⊕A0'B1⊕A1'A0'

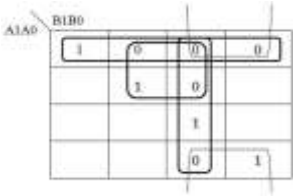


Fig.27: Exorlink k-map for A=B

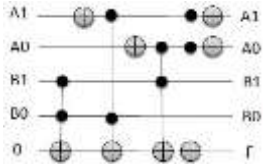


fig.28: Exorlink Reversible Circuit for A=B

Quantum Cost: 4*5 + 4 = 24

A<B:

DSOP:F=A1'B1⊕A1'A0'B1'B0⊕A1A0'B1B0

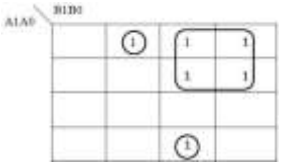


Fig.29: DSOP k-map for A<B

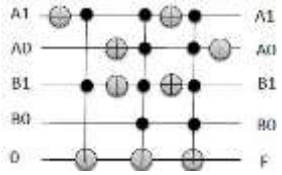


fig.30: DSOP Reversible Circuit for A<B

Quantum Cost: 2*29 + 5 + 6 = 69

Exorlink: F=A1'A0'B0⊕A1'B1⊕A0'B1B0

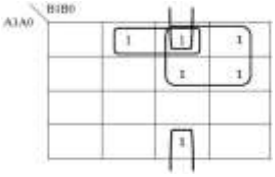


Fig.31: Exorlink k-map for A<B

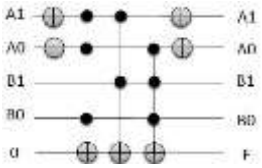


fig.32: Exorlink Reversible Circuit for A<B

Quantum Cost: 2*13 + 5 + 4 = 35

Table.6: Total Quantum Cost for Comparator

Comparator	Total Quantum Cost
DSOP Reversible Circuit	69+124+69=262
Exorlink Reversible Circuit	35+24+35=94

Thus it can be seen that there is an enormous decrease in the Quantum Cost for Exorlink when compared to DSOP. Hence Exorlink is the most powerful operation which can link any two cubes in an array of cubes of an arbitrary distance. Functions realized by Exorlink can have fewer gates, fewer connections and less Quantum Cost when compared to the DSOP logic.

V CONCLUSION

Exorlink logic employed in the combinational circuits like full adder, full subtractor, comparator, etc. proves to be the most powerful operation in Reversible logic synthesis. It can link any two cubes in an array of cubes of an arbitrary distance. By using this logic, number of variables in the expression gets minimized, thereby reducing the Quantum Cost compared to the Disjoint- Sum of Products (DSOP). Employing Reversible Logic and optimizing the Quantum Cost by using Exorlink technique reduces the heat dissipation in the circuits which leads to new approach for Integrated Circuit design and help in continuing Moore's Law.

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