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# RESILIENT ERROR CONTROL METHODS FOR NETWORK ON CHIP TWO FOLD LAYERS

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## Abstract

In this work, we propose a dual-layer cooperative error control framework, which includes the application of an adaptive error control coding method and a simple configurable routing algorithm. The proposed dual-layer framework facilitates the congestion-aware error control in NoCs. When the network layer detects an increase in network congestion caused by the employed error control scheme, either routing algorithm or error control strength is changed to reduce the congestion, depending on the stress value of the intended buffers. As channel noise increases, the adaptive error control in the data link layer is switched to a more powerful error control mode, cooperating with the configurable routing algorithm.

**Keywords:** Dual layer, cooperative error control, congestion aware,

## Introduction

With the development of integration technology, System on-Chip (SoC), composed of heterogeneous cores on a single chip, has entered billion-transistor era. As the device geometry shrinks toward the nano meter scale and current System-on-Chips (SoC) integrate 10 to 100 or more of embedded functional units and storage blocks, the interconnection between these blocks became the bottle neck in achieving high degree of integration, to solve that problem the researchers introduced Network-on-Chips (NoC) as a way to achieve a high degree of integration and performance requirements. Network on chips are highly exposed to several sources of transient noise, affecting signal integrity and system reliability. As a result, error control and recovery schemes have been discussed.

On-chip communication becomes more susceptible to crosstalk, external radiation and spurious voltage spikes; thus, efficient methods are needed to tackle the increasing reliability problem in Network on Chips. As shown in Fig. 1(b) and Fig. 1(c), error control coding (ECC) modules are typically employed in the input and output channels of a router to detect/correct errors existing on the received data.

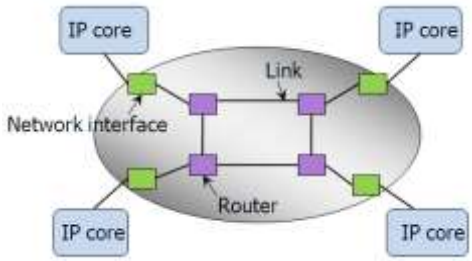
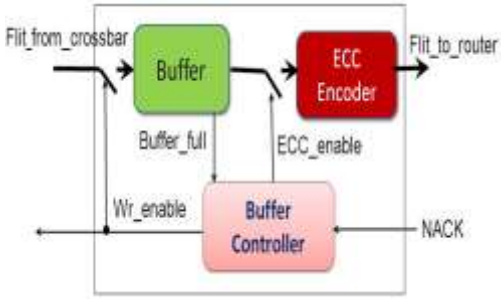
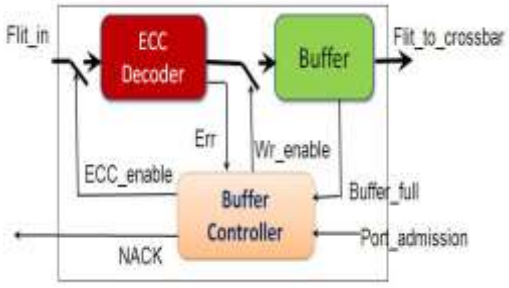



Figure.1 (a) Simplified view of a network-on-chip (NI: Network interface; R: Router)




b) Input channel




c) Output channel

The data link-layer or network-layer ECC methods are suitable for different noise regions and route lengths. To consider a wide range of operating environments and the associated overhead costs, we propose a framework that can adapt ECC strength across data link and network layers to improve reliability and energy efficiency while maintaining performance.

The remainder of this paper is organized as follows.

In Section II, we provide dual layer error control frame work.

The application of product codes to the dual-layer ECC codec is described in Section III.

Experimental results are presented in Section IV.

Conclusions are provided in Section V.

## Section II:

### Dual-layer Error Control Framework with ECC Encoder and Decoder.

We propose a dual-layer error control framework facilitating cooperative data link/network adaptive error control, to manage errors in varied noise conditions while simultaneously adjusting for network congestion. Fig. 2 depicts our concept of dual-layer cooperative error control. The Packetization unit (network layer) divides packets from the IP cores into flits (flow control units) for transmission.

The Depacketization unit (network layer) assembles and orders flits into packets to deliver to IP cores. The Congestion Control module (network layer) analyzes feedback from error detection and the router buffer status to judge the network congestion. Then, the congestion control determines an appropriate routing algorithm for the network layer and selects an energy-efficient error control scheme for the data link layer. The Adaptive ECC Encoder/Decoder (data link layer) implements hardware-efficient adaptive error detection/correction codes.

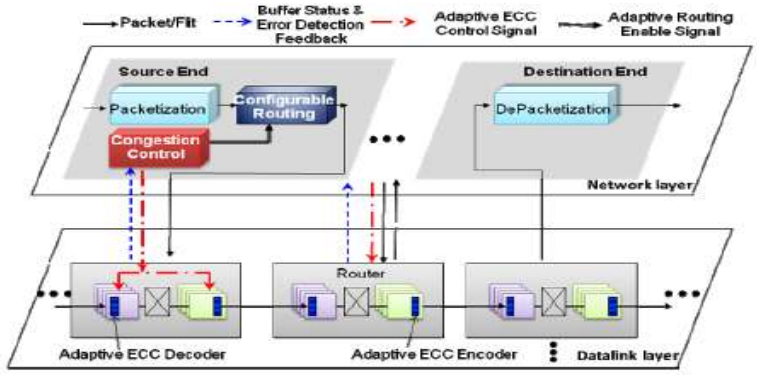



**Fig 2: Dual Layer Technique**

## Proposed ECC mode Switching method

### a. ECC mode switching protocol

In variable noise conditions, cooperation of end-to-end and hop-to-hop ECC improves energy efficiency and performance. We propose an ECC mode switching protocol to facilitate error control cooperation at runtime. End-to-end ECC in the network layer (i.e., single-layer mode) is used in low noise conditions while end-to-end ECC and hop-to-hop ECC (i.e., dual-layer mode) are used in high noise conditions.

### b. Dual-Layer Information Exchange

In the proposed method, the mode switching depends on the information exchange between data link and network layers. In mode 1 (end-to-end ECC), the network interface assesses the global noise condition by counting the number of errors detected by the destination decoder, and informs the data link layer if it should use hop-to-hop ECC . In mode 2 (end-to-end ECC combined with hop-to-hop ECC), the network interface comprehensively evaluates the global noise condition with its local error counter and information passed by the error history flit, which is filled by the EHF Update Unit in the data link layer.

## Dual-Layer ECC Encoder

The end-to-end ECC encoder is located in the network interface. Fig. 3 shows the encoding process and encoder architecture. The binary bit stream of each packet is arranged into an array where each flit is a column.

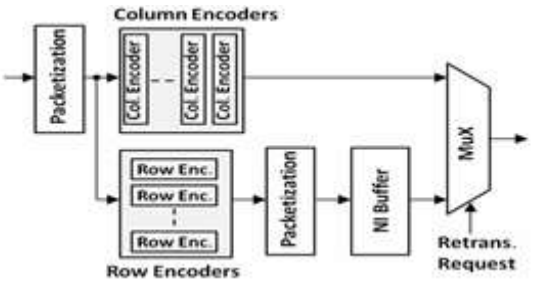



**Fig 3: Dual Layer ECC Encoder**

## Dual-Layer ECC decoder

The dual-layer ECC decoding process is shown in Fig. 4. In the decoding process, the flit belonging to the first packet transmission is decoded with a column decoder. If the first packet transmission has a detectable but uncorrectable error, a short NACK packet with opposite source/destination address is created to request transmission of the PCB and Coded packet; meanwhile, the coded packet and column error vector are stored in the network interface buffer. Otherwise, the uncoded data packet is delivered to the associated IP core.

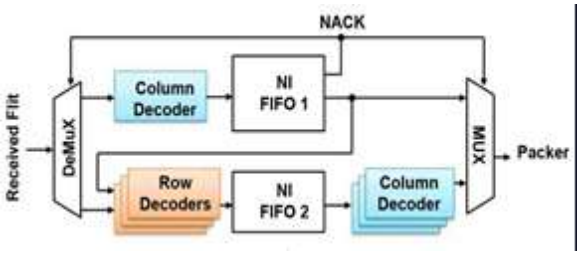



**Fig 4: Dual Layer ECC Decoder**

## Section III:

### Adaptive Error Correction Coding for NoC

As Networks-on-Chips (NoCs) continue to become more susceptible to process variation, cross-talk, hard and soft errors with technology scaling to sub-nanometer, there is an urgent need for **Adaptive Error Correction Coding** (ECC) schemes for improving the resiliency of the system.

The goal of adaptive ECC schemes should be two fold; decrease power consumption when errors are infrequent, thereby maximizing power savings and increase the fault coverage when errors are frequent, thereby improving application speedup while consuming more power.

Here we propose an energy-efficient error control scheme for on-chip interconnects capable of correcting a combination of multiple random and burst errors. The iterative decoding method, inter leaver, using two-dimensional Hamming product codes and a simplified type-II hybrid ARQ, achieves several orders of magnitude improvement in residual flit-error rate for multi wire errors and up to 45% improvement in throughput in high noise environments. For a given system reliability requirement, the proposed error control scheme yields up to 50% energy improvement over other error correction schemes. The low overhead of our approach makes it suitable for implementations in on-chip interconnect switches.

Error protection can also be incorporated in the routing algorithm at the network layer for higher performance. For efficiency dynamic routing algorithms manage the faulty links and nodes by providing multiple path choices.

### Analysis of Error Control Schemes for On-chip Interconnect

Error control methods have been widely investigated at the data link layer. The proposed error-control coding to balance power and reliability in deep submicron (DSM) SoCs it is implemented in the dual layer.

We proposed configurable error correction; implemented and evaluated this adaptation using a hardware sharing technique for reduced area and energy overheads in variable noise conditions.

### Hop-to-hop Error Control

In the widely used packet-based communication, each packet consists of data units called flits. Hop-to-Hop ECC is performed in the data link layer, the flits are encoded and decoded for error correction/detection in each hop of the transmission from the sender to the receiver. Merits and demerits are as follows.

1) Hop to hop method detects error and recovers within current hop.

2) It prevents error accumulation.

3) It adds complexity to router design.

### End-to-End error control

End-to-end error control typically is performed on the entire packet in source/destination end. An acknowledge packet is sent back to the source end to request retransmitting the packet Network-layer error control coding is executed only in the network interface and does not detect or correct errors at intermediate hops in the route. Merits and demerits are as follows.

1) Error control does not increase router complexity.

2) Power consumption is less than that of hop-to-hop error control.

**Evaluation of the Proposed Error Control Scheme in multi layer NoC.**

Single-error correcting (SEC) codes and parity-based detection schemes were explored. Forward error correction (FEC) directly corrects the captured errors without requiring retransmission and increasing congestion; however FEC is typically designed for worst-case noise conditions, where energy consumption is more. In contrast, hybrid ARQ trades off network congestion and energy consumption by only retransmitting the flits that contains errors beyond the error correction capability provided in the receiver.

To obtain a wide adaptation range of error resilience, we construct an M-error correcting, 2M-error detecting (MEC-2MED) code to facilitate adaptive error detection and correction.

Arbitrarily combining an error detection code with an error correction code will result in a prohibitive overhead. To reduce the cost, we overlap the error detection and correction codec circuits, by using multiple sets of extended Hamming codes and linear block interleaving. Extended Hamming is capable of detecting and correcting simultaneously; thus, it is a good basis for our MEC-2MED code.

Three error detection and correction modes are achievable—**SEC-DED** using EHM(72,64)(shortened from an extended Hamming(128,120)), double-error correction, four-bit error detection (DEC-4ED) EHM(78,64) using two groups of EHM(39,32) (shortened from an extended Hamming(64,57)); four-bit error correction, eight-bit error detection (4EC-8ED)EHM(88, 64) using four EHM(22,16) (shortened from an extended Hamming(32,26)).

A set of M SEC codes are able to recover M-bit errors, as long as those M erroneous bits are properly distributed to the input of M SEC decoders. Multiple SEC codecs combined with linear block interleaving can achieve multi-bit error correction, with reduced hardware compared to other multiple error correction schemes, suchas Bose-Chaudhuri-Hocquenghem (BCH) and convolutional codes.

## Performance Analysis of Recovery Schemes on NoC's

The various error control schemes have different strengths. In ARQ, the error detection codes are easy to construct at a minor energy cost; however, retransmission reduces throughput (especially in a persistent noise environment) making it unsuitable for high performance applications. FEC can guarantee a certain throughput, but powerful error correction codes are more complex and consume large energy.

Cyclic redundancy check (CRC) codes are used to detect errors, and retransmission is used once errors are detected. Instead of CRC, Hamming codes are used to detect two single errors or to correct a single error single-error correcting double-error detecting (SEC-DED) codes (e.g., extended Hamming) are used to perform HARQ. In order to improve error resilience against burst errors, interleaving can be used.

The simplest two-dimensional product codes are single parity check (SPC) product codes, guaranteed to correct only one error by inverting the intersection bit in the erroneous row and column. Multidimensional SPC product codes can be constructed to improve the error correction capability, but a more complex decoding process is required.

Direct implementation of product codes results in low code rates (because of the large number of redundancy bits) and increased link energy consumption. In order to improve code rate and achieve energy efficiency, we use a modified type-II HARQ, in which redundancy bits are incrementally transmitted when necessary, combined with an iterative decoding method to process Hamming product codes.

**Fig 5: CRC Existing Method**

Among several error correction schemes like Hamming, BCH, and Reed-Solomon codes where Hamming codes are the most widely used codes in NoC error protection. In this section, Hamming code is discussed as one example of error correction coding approaches and its capability to correct single and burst errors. Its special is that this technique can easily be implemented in hardware and the code is corrected before the receiver knows about it.

We present hardware performance analyses of Hamming product codes combined with type-II hybrid automatic repeat request (HARQ), for on-chip interconnects. in a network-on-chip environment. The method of combining Hamming product codes with type-II HARQ achieves several orders of magnitude improvement in residual flit error rate. For a given residual flit error rate requirement (e.g., $10^{-20}$), this method yields up to 50% energy improvement over other error control methods in high-noise conditions.

## Discussions

One of the main concerns in on-chip communication is the throughput. This is also one of the good features of the FEC scheme, since no time consuming retransmissions are needed. The circuit realizations show a huge variation in throughput.

The power consumption is an important criterion in designing on-chip communication. Here In this work we have concentrated on the encoder/decoder circuits while a complete analysis should take into consideration in future research. Consequently, even without provision of retransmission the probability of data loss will be negligible. This suggests that higher order error correcting codes will be more area efficient than retransmission-based mechanisms.

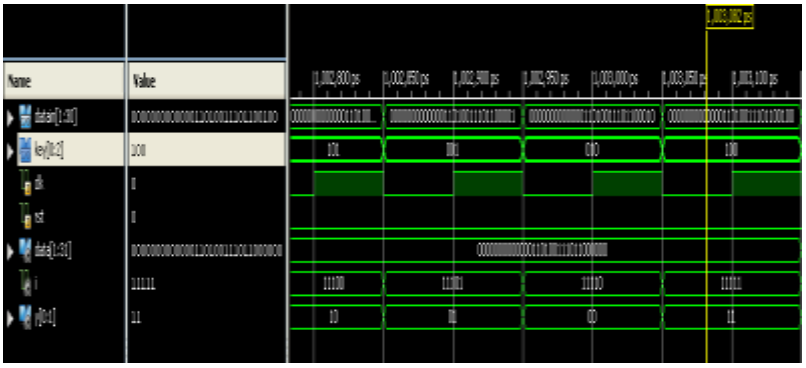


**Fig 6: CRC Proposed Method**

CRC a very effective error detection method can detect, with a very high probability, all burst errors.

## Comparative studies: Hamming Codes and CRC with results.

Unlike the Hamming code, CRC code a effective error detection method exhibits the additional feature to target both random error patterns and error bursts with high probability. A Hamming code relies on its capability to detect multiple errors arbitrarily located all over the codeword, while CRC code is particularly suitable to deal with errors affecting lines that are close to each other (within the detectable burst length). With respect to the application to on-chip reliable communication, CRC code is effective whenever the communication failure mechanism affects a certain number of contiguous lines.

On the contrary, Hamming codes can be efficiently used whenever errors are spread all over the bus and the detection of error patterns is more effective than that of error bursts Both CRC4 and CRC8 can detect single errors and any odd number of errors .We opt for the worst-case assumption that they can detect only single and burst errors, which is usually enough to motivate the adoption of CRC codes from a practical viewpoint.

In order to accurately assess efficiency of linear codes used to span the energy–reliability tradeoff for on-chip communication links, we proceeded with the synthesis of encoder and decoder for the considered coding schemes and for a 32 bit link, coming up with the results reported in Table I. In addition, a simple single parity bit code (PAR) is considered for comparison, as it involves minimum redundancy in terms of link lines (only one check bit). Its detection capability includes all errors in an odd number of bits.

All of the error control schemes use retransmission as error recovery strategy, except for SEC and SECDED that correct single errors. A 0.25- m synthesis library has been used, with a supply voltage of 2.5 V.

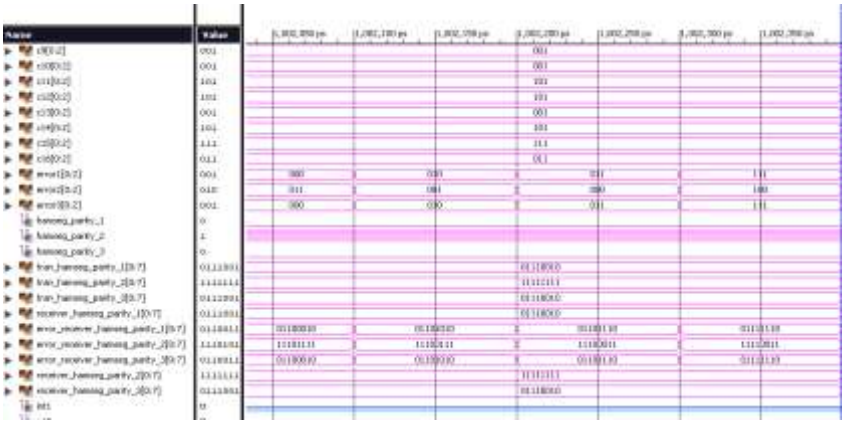


**Fig 7: HAMMING 1D Method**

It can be observed that CRC codes exhibit the most lightweight implementations, comparable to that of a single parity check code. Area and power metrics for CRC4 and CRC8 are sometimes counterintuitive, because the final circuit realization is strongly dependent on the generator polynomial.

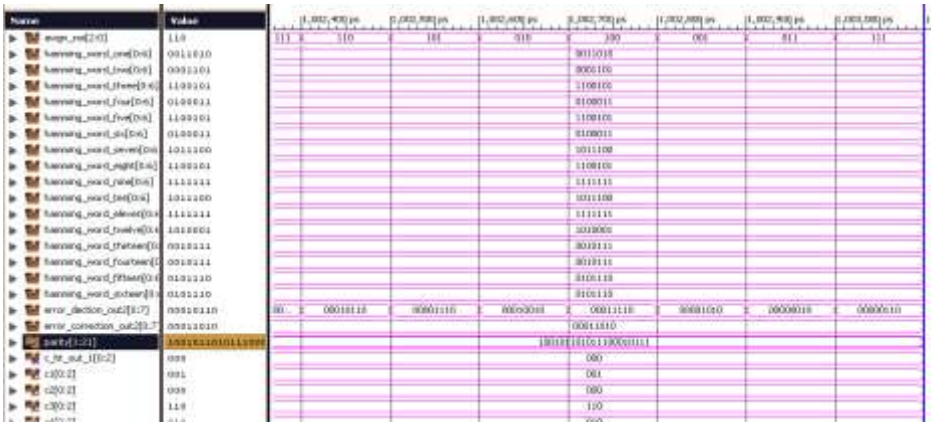


**Fig 8: HAMMING 2D Method**

DSM technologies are particularly sensitive to these effects, in that the shrinking of geometries makes the relative distance between interconnects smaller, therefore even localized noise sources are likely to have an impact on multiple contiguous bus lines.

### Simulation

Minimal power consumption for the codecs have been obtained by means of back-annotation of switching activity of gates' internal nodes from very high speed hardware language (VHDL) simulation.

Note that VHDL simulation is performed (for all codes) for the different cases of reliable communication: which runs error free. In order to implement these codes, we require an encoder at the sender and a decoder at the receiver of the bus. Consequently, we modelled the encoders and decoders **SEC-DED** using EHM in VHDL.

## Comparison Table

| Error correction method | One dimensional | Two dimensional | Available |
|---|---|---|---|
| Number of Slice Flip Flops | 6 | 4 | 3840 |
| Number of 4 input LUTs | 88 | 77 | 3840 |
| Number of IOs | 253 | 253 | |
| Number of bonded IOBs | 253 | 229 | 141 |
| Total REAL time to Xst completion | 10.00 secs | 9.00 secs | |
| Total CPU time to Xst completion | 9.81 secs | 8.34 secs | |
| Total memory usage | 189450kilobytes | 136160 kilobytes | |

## Conclusion

Future digital systems implemented with nanoscale technologies are very sensitive to errors emerging from various sources. In order to construct a reliable and fault tolerant robust system, efficient error correction methods are needed. In this paper, different error correction schemes for nano scale network-on-chip were studied and analyzed in terms of error correction capability, power consumption, throughput and area. The focus was on error scenarios where several single error and burst errors that could occur simultaneously and independently of each other. Errors recovery schemes can significantly decrease the power consumption by 20% for a given error rate and performance.

It was shown that the complex error control methods, were efficient but the drawback was larger area and reduced throughput. As verified through detailed analysis and simulations, the proposed scheme lowers the energy dissipation compared to all other existing schemes studied here.

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