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VLSI IMPLEMENTATION OF HIGH QUALITY IMAGE SCALING PROCESSOR

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Abstract: A low-complexity, low-memory requirement, and high-quality algorithm is proposed for VLSI implementation of an image scaling processor. The proposed image scaling algorithm consists of a sharpening spatial filter, a clamp filter, and a bilinear interpolator. To reduce the blurring and aliasing artefacts produced by the bilinear interpolation, the combination of spatial and clamp filters which is called as combined filters are added as pre-filters. The hardware cost of the combined filters can be reduced by using reconfigurable calculation unit. This work reduces gate counts and requires only a one-line-buffer memory. The Spurious Power Suppression Technique (SPST) is used here to reduce the power. It separates the target design into two parts i.e., the most significant part(MSP) and last significant part(LSP), and turns off the MSP when it does not affect the computation results to save the power. The SPST proposes an original glitch-diminishing technique to filter out useless switching power by asserting the data signals after the data transient period. It is used in Multimedia and DSP applications.

Keywords: Image scaling, Bilinear Interpolator, SPST.

I INTRODUCTION

Image scaling is the process of resizing a digital image. It has been widely applied in the fields of digital imaging devices such as digital cameras, digital video recorders, digital photo frame, high-definition television, mobile phone, tablet PC, etc. An obvious application of image scaling is to scale down the high-quality pictures or video frames to fit the minimize liquid crystal display panel of the mobile phone or tablet PC. As the graphic and video applications of mobile handset devices grow up, the demand and significance of image scaling are more and more outstanding. The image scaling algorithms can be separated into polynomial-based and non-polynomial-based methods. The simplest polynomial-based method is a nearest neighbour algorithm. It has the benefit of low complexity, but the scaled images are full of blocking and aliasing artefacts. The most widely used scaling method is the bilinear interpolation algorithm by which the target pixel can be obtained by using the linear interpolation model in both of the horizontal and vertical directions.

II RELATED WORK

A novel scaling algorithm is proposed for the implementation of 2-D image scalar. The clamp and sharpening spatial filters are added as pre-filters to solve the blurring and aliasing effects produced by bilinear interpolation. Furthermore, an adaptive technology is used to enhance the effects of clamp and sharpening spatial filters. To reduce memory buffers and computing resources for the very large scale integration (VLSI) implementation, the clamp filter and sharpening spatial filters both convoluted by a 3×3 matrix coefficient kernel are combined into a 5×5 combined convolution filter. An edge-oriented area-pixel scaling processor is to achieve the goal of low cost, the area-pixel scaling technique is implemented with low-complexity VLSI architecture. A simple edge catching technique is adopted to preserve the image edge features effectively so as to achieve better image quality Compared with the previous low-complexity techniques; it performs better in terms of both quantitative evaluation and visual quality.

An efficient VLSI design of bi cubic convolution interpolation for digital image processing. The architecture of reducing the computational complexity of generating coefficients as well as decreasing number of memory access times. Numerous digital image scaling techniques have been presented. The most popular methods are nearest neighbour, bilinear, Win scale, bi-cubic, and cubic. In which the simplest approaches are nearest neighbour and bi-linear interpolation. A better quality of interpolation is achieved by using higher order models. The high-speed VLSI architecture has been successfully designed with high performance architecture of bi-cubic convolution interpolation.In this paper bilinear interpolation technique is used for designing image scaling processor which has got the advantage of reducing the computing resources, memory requirement and it can be easily implemented in VLSI.

III PROPOSED SYSTEM

It consists of a sharpening spatial filter, a clamp filter, and a bilinear interpolation. The sharpening spatial and clamp filters serve as pre-filters to reduce blurring and aliasing artifacts produced by the bilinear interpolation. First, the input pixels of the original images are filtered by the sharpening spatial filter to enhance the edges and remove associated noise.

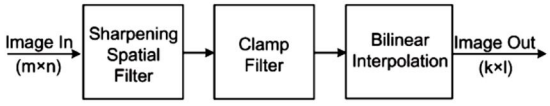


Figure 1 Block diagram for proposed scaling algorithm

Second, the filtered pixels are filtered again by the clamp filter to smooth unwanted discontinuous edges of the boundary regions. Finally, the pixels filtered by both of the sharpening spatial and clamp filters are passed to the bilinear interpolation for up or downscaling. To conserve computing resource and memory buffer, these two filters are simplified and combined into a combined filter.

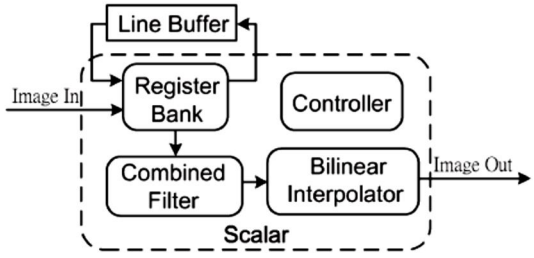


Figure 2 Block diagram of VLSI architecture

The proposed scaling algorithm consists of two combined prefilters and one simplified bilinear interpolator. For VLSI implementation, the bilinear interpolator can directly obtain two input pixels *P*_ (m ,n) and *P*_ (m,n+1) from two combined prefilters without any additional line-buffer memory. The above Figure 2 shows the block diagram of the VLSI architecture for the proposed design. It consists of four main blocks: a register bank, a combined filter, a bilinear interpolator, and a controller. The details of each part will be described in the following sections.

Image scaling Processor can be separated into polynomial-based and non-polynomial-based methods. The simplest polynomial-based method is a nearest neighbour algorithm. It has the benefit of low complexity, but the scaled images are full of blocking and aliasing artefacts. The most widely used scaling method is the bilinear interpolation algorithm, by which the target pixel can be obtained by using the linear interpolation model in both of the horizontal and vertical directions. The high-quality image scaling algorithms have the characteristics of high complexity and high memory requirement, which is not easy to be realized by VLSI technique. Thus for real-time applications, low-complexity image processing algorithms are necessary for VLSI implementation.

ARCHITCTURE OF RCU

The RCU is designed for producing the calculation functions of (S-C) and (S-C-1) times of the source pixel value, which must be implemented with C and S parameters. The C and S parameters can be set by users according to the characteristics of the images. The architecture of the proposed low-cost combined filter can filter the whole image with only a one-line-buffer memory, which successfully decreases the memory requirement from four to one line buffer of the combined filter. The Figure 4 shows the six-stage pipelined architecture of the combined filter and bilinear interpolator, which shortens the delay path to improve the performance by pipeline technology.

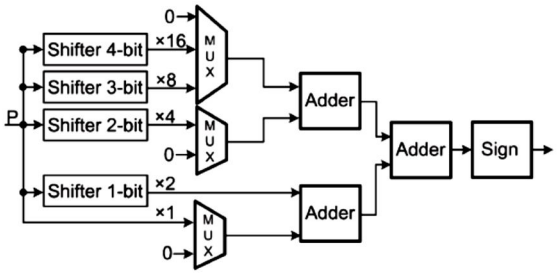


Figure 3 Architecture of RCU

The stages 1 and 2 in Figure 5 show the computational scheduling of a T-model combined and an inverse T-model filter. The T-model or inversed T-model filter consists of three reconfigurable calculation units (RCUs), one multiplier–adder (MA), three adders (+), three subtracters (−), and three shifters (S).

BILINEAR INTERPOLATOR

The bilinear interpolation is an operation that performs a linear interpolation first in one direction and, then again, in the other direction. It is the mainly selected because of its characteristics with low complexity and high quality.

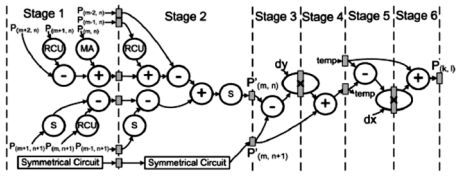


Figure 4 Computational Scheduling

The output pixel *P*(k,l) can be calculated by the operations of the linear interpolation in both *x*- and *y*-directions with the four nearest neighbour pixels, where *P*(m,n), *P*(m+1,n), *P*(m,n+1), and *P*(m+1,n+1) are the four nearest

neighbour pixels of the original image and the dx and dy are scale parameters in the horizontal and vertical directions. The simplifying procedures successfully reduce the computing resource from eight multiply, four subtract, and three add operations to two multiply, two subtract, and two add operations.

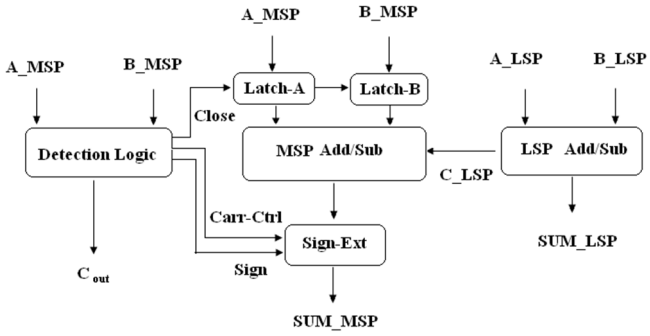


Figure 5 Block Diagram of SPST Technique

The proposed SPST separates the target designs into two parts, i.e., the most significant part and least significant part (MSP and LSP), and turns off the MSP when it does not affect the computation results to save power. The SPST proposes an original glitch-diminishing technique to filter out useless switching power by asserting the data signals after the data transient period. The proposed design is applied to two multimedia/DSP design examples, i.e., a multi transform design for H.264 and a versatile multimedia functional unit (VMFU).

IV SIMULATION RESULTS

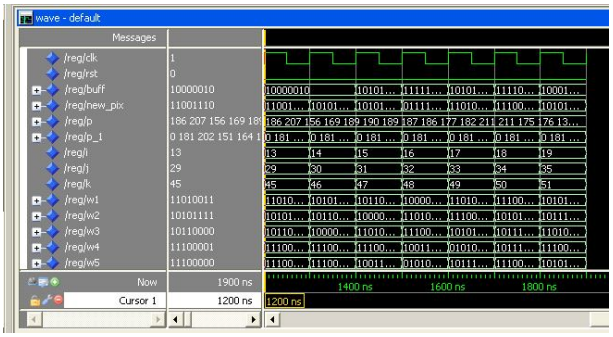
To be able to analyse the qualities of the scaled images by various scaling algorithms, a peak signal-to-noise ratio (PSNR) is used to quantify a noisy approximation of the refined and the original images. Since the maximum value of each pixel is 255, the PSNR expressed in dB can be calculated as

$$PSNR = 10\log_{10}\frac{MN \times 255^2}{\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}[P(i,j)| - P'(i,j)]^2}$$

Where M and N are the width and height of the original image.

Input Image

Output Image



VLSI Output Waveform

V CONCLUSION

A low-cost, low-memory-requirement, high quality and high-performance VLSI architecture of the image scaling processor had been designed. The filter combining, hardware sharing, and reconfigurable techniques had been used to reduce hardware cost. It reduces the gate count up to 34.5 and requires only one-line memory buffer.

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