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PROBABILISTIC BASED LOW POWER NOISE TOLERANT LATCH DESIGN

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Abstract

In this paper an ultra low power and probabilistic based noise tolerant latch is proposed based on Markov Random Field (MRF) theory. The absorption laws and H tree logic combination techniques are used to reduce the circuit complexity of MRF noise tolerant latch. The cross coupled latching mechanism is used at the output of the MRF latch in order to preserve the noise tolerant capability of MRF latch. The proposed latch is faster than the latches presented in the literature and provides low power and high noise immunity. Hence we can achieve good trade off in terms of performance, robustness and cost. The latches are evaluated in 180nm CMOS technology. The results obtained show that the proposed latch consumes low power and highly noise tolerant..

Keywords*:* Markov Random Field (MRF) latch, Markovian Property, C-element, Single Event Upset (SEU), Soft error tolerant, Root Mean Square (RMS) noise voltage.

1. Introduction

CMOS technology is approaching the nano-electronics range nowadays, but experiences some practical limits. High dynamic power dissipation and leakage current in deep submicron technologies contribute a major proportion of total power dissipation in CMOS circuits designed for portable applications. Today, there are an increasing number of portable applications requiring small-area, low-power and high-throughput circuitry .Lowering the supply voltage appears to be the most well known means to reduce power consumption. Power consumption has become one of the biggest challenges in high-performance logic circuit design. Designers are thus continuously challenged to come up with innovative ways to reduce power[4], while trying to meet all the other constraints imposed on the design. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. The lower threshold voltage will cause a decrease in noise-tolerance. Moreover, noise does not scale down proportionally as supply voltage decreases. As the size of CMOS devices continues to scale down to the nanometer scale, signal errors caused by noise can significantly affect the circuit performance. The circuits operate at low noise margins and thus VLSI circuits are more sensitive to noise [1-3]. The MRF approach is further extended to the design of a probabilistic-based noise-tolerant sequential circuit in this paper.

2 .Sequential Circuits

Sequential circuits are classified into latches and flip-flops, where flip-flops are edge triggered sequential circuits and latches are level sensitive sequential circuits. When the noise affects the input signal, the latch will be affected during the entire transparent period while the flip-flop will be affected during the clock transition edge. Hence, the latches are mostly affected by noise than flip-flops. Hence, latches are inherently more susceptible to noise interference. In order to minimize the effect of noise interference and allow the circuit to operate reliably under low-voltage, low power, and low-SNR environments, we propose a noise-tolerant latch design by using Markov Random field (MRF) theory [1].

2.1 Mux Based Latch Circuits

In the Multiplexer-based latch Fig 1, MUX-Latch [1], the CLK signal acts as the switch. When CLK is at logic low, the latch is in latching mode and its output remains unchanged. When CLK is at logic high, the latch circuit enters into transparent mode, where its output logic state is determined by its input signal [6]. The noise interference at the input affects the correctness of the output state when the latch is in the transparent mode. The circuit complexity is less but requires more transistors and delay is more. In Two Transmission Gate-Latch Fig 2 the charging and discharging period is reduced as the clk frequency increases. In the transmission gate cross-coupled feedback inverter latch Fig 3, the operational speed is slightly increased and the power consumption is slightly reduced. The main drawback is when the input is switching in the transparent mode, the contention between the feedback signal and the feed forward input signal will cause additional operational delay and more power consumption.

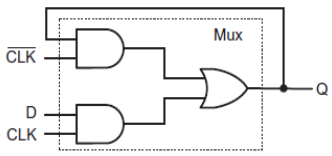


Figure 1: Mux Based Latch

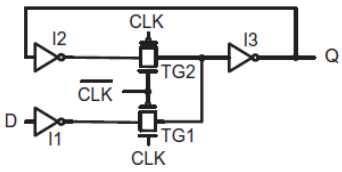


Figure 2: Transmission Gate based Latch

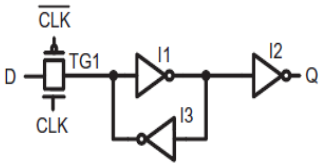
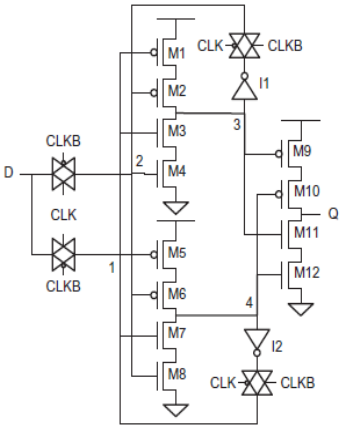
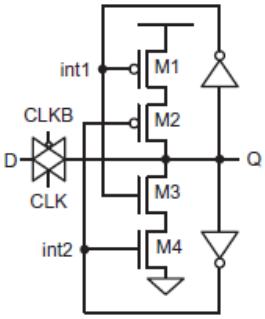


Figure 3: Transmission gate Cross coupled latch

2.2 Soft Error Tolerant Latch Designs

The soft errors are due to internal and externally induced phenomena such as a particles and cosmic rays in adverse environments during system operation; this is especially deleterious for storage elements, such as flip-flops, latches. To reduce the impact of a soft error on latches, hardening techniques have been utilized. Soft-error tolerant latch designs with increased soft error upset tolerance capability such as Feedback Redundant SEU-Tolerant Latch (FERST) Fig 4,Split Internal Low Cost latch[4] (SIN-LC) Fig 5 and HiPeR latch design [5] Fig 6 are discussed . These latest designs can perform with superior noise-tolerance for soft-error. Since soft errors are usually one shot noise they cannot resist continuous noise interference which leads to the destruction of the C-element. As a result, for the noise interference with multiple error cases, the output or of these latch designs may be malfunction. The hardware complexities of these latch designs are usually higher, as more transistors are required for the construction of the C-element.





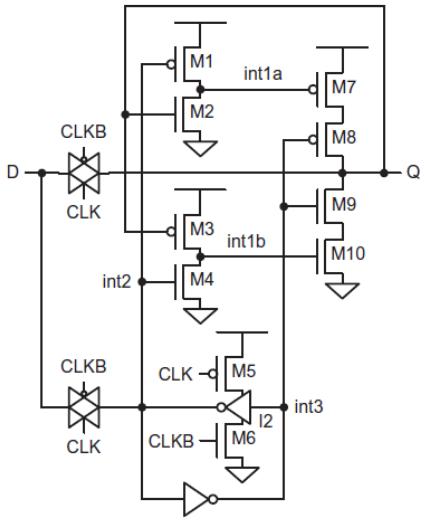


Figure 4: FERST Latch **Figure 5:** SIN-LC Latch **Figure 6:** HiPer Latch

3. MARKOV RANDOM FIELD (MRF) THEORY

The MRF approach can express arbitrary logic circuits and the logic operation is achieved by maximizing the probability of correct state configurations in the logic network depending on the interaction of neighbouring circuit nodes. The computation proceeds via probabilistic propagation of states through the circuit. Crucially, the MRF logic can be implemented in modified CMOS-based circuitry that trades off circuit area and operation speed for the crucial fault tolerance and noise immunity. Hence a new approach to the design and operation of logic circuits where the logic states are considered to be random variables are proposed. Under this framework, one no longer expects a correct logic signal at all nodes at all times, but only that the joint probability distribution of signal values has the highest likelihood for valid logic states[7]. A model for the MRF is a graph structure, where the nodes of the graph represent logic variables and the edges represent statistical dependency between the variables.

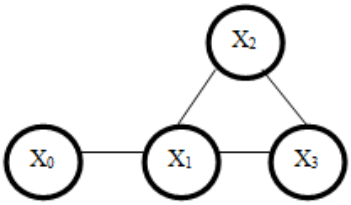


Figure 7: MRF Model

An appropriate model for the MRF is a graph structure, where the nodes of the graph represent logic variables and the edges represent statistical dependency between the variables. An example of such a graph is shown in Figure 1 for a very small logic circuit. There are four logic variables represented by the vector {x0, x1, x2, x3} and these variables are the nodes of the graph in the lower half of the Fig 7. The edges of the graph indicate

that the subsets of nodes {x0, x1},{x1,x2,x3} directly interact. These subsets are called cliques from the graph theory concept of node subsets that are all mutually connected by graph edges [8]. For any MRF graph G there exists a set of cliques C that represent the local statistical dependencies of logic states. The distribution of noise energy can be spread and shared among these MRF neighbouring nodes. The noise-tolerant capability is achieved in a MRF network through iteratively updating the logic states of each individual node. Ultimately the network converges to a stable set of state, which corresponds to the correct logic states of each node. It is worth mentioning that successful operation in an MRF network model only requires that the energy of correct states is lower than the energy of incorrect states which can therefore easily be achieved.In[8], the hardware complexity in constructing an MRF logic gate is reduced through Boolean simplification and valid minterm reduction. Mapping the MRF logic gate by using the simplified Boolean equation in the circuit can greatly reduce the area.

3.1 Markov Random Field (MRF) Latch

Based on this idea, MRF latch Fig 8 was designed with low power and high noise immunity. The circuit complexity is reduced using absorption law and H tree balanced logic circuit merging method. After H-tree combination these cascaded logical gates with the same type, will lower the influence of noise in each MRF network node and reduce the current charging/discharging paths. It is beneficial to enhance both noise tolerance and power consumption. With the cross-coupled latching mechanism design, the conduction of transistors will become a collaborative decision together with the two added transistors n1 and n2 and no longer be reliant on only a single transistor. The conduction of transistors n1 and n2 are decided by the complementary cross-coupled feedback signals, the possibility of direct conduction of the transistors is greatly reduced [1]. This results in the reduction of noise tolerance and power consumption in MRF latch. When CLK = 1, the latch circuit is in transparent mode, where the latch's output Q is directly determined by its input D. When CLK = 0, the latch circuit is in latching mode, where the latch's output Q is latched the same as its previous state Q2. The operation mode of a latch is mainly controlled by the CLK signal.

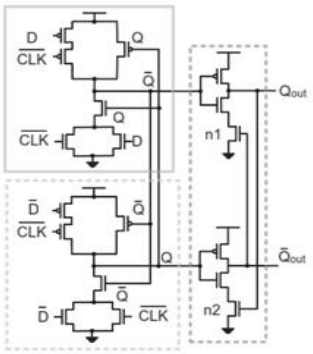


Figure 8. Proposed MRF Latch

4. RESULTS AND COMPARISION

The Table I exhibits performance of all the existing latches and proposed latch in terms of delay, area and power, RMS noise voltage. The results show that the proposed MRF latch provides better noise tolerance and low power compared to the existing latches.

TABLE I

PERFORMANCE OF THE PROPOSED MRF LATCH COMPARED WITH PREVIOUS IMPLEMENTATIONS

LATCHES	POWER	AREA	DELAY	RMS INPUT NOISE VOLTAGE	RMS OUTPUT NOISE VOLTAGE
MUX based latch	3.116nw	377 μm^2	3.000 ps	34.732V	42.739V
TG based mux latch	2.833uw	273 μm^2	207.95ps	35.812V	48.066V
TG cross coupled latch	8.112uw	276 μm^2	366.60ps	35.313V	39.049V
FERST latch	5.639nw	780 μm^2	9.8711ns	29.756V	30.498V
Sin-LC latch	10.759nw	216 μm^2	64.471ps	36.678V	38.408V
Hiper latch	282.91uw	546 μm^2	10.303ps	32.921V	33.140V
MRF latch	0.9487nw	588 μm^2	662.31ps	41.427V	23.603V

5. CONCLUSION

In this paper a low power noise tolerant Markov Random Filed latch design is proposed. In TSMC 180 nm CMOS process, the proposed circuit can operate reliably under low power and superior noise tolerance as compared with the conventional CMOS latch design. Through MRF mapping decomposition, MRF theory is applied to sequential noise tolerant circuits. By applying the absorption law and H-tree logic combination techniques to simplify MRF noise-tolerant latch circuit, the circuit complexity and power consumption was reduced. By applying the cross-coupled latching mechanism in the output of MRF latch, the noise tolerance of MRF latch was preserved. Hence the Markov Random Field (MRF) latch consumes low power and highly noise tolerant compared to all the existing latches.

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