INTERNATIONAL JOURNAL OF RESEARCH IN COMPUTER APPLICATIONS AND ROBOTICS
ISSN 2320-7345

DESIGN OF MODIFIED DECODER FOR CONCURRENT BIST ARCHITECTURE

Surenkosimin.M[1], Kalimuthu.T[2]

[1] PG SCHOLAR DEPT.OF VLSI DESIGN, *Scad College of engineering and technology,padmasuren@gmail.com*
[2] ASSISTANT PROFESSOR DEPT.OF ECE (UG), *Scad College of engineering and technology,kalimuthu.t@gmail.com*

Abstract

Design of MDEC concurrent Built-in self test (BIST) designed for self testing process chip (or) circuit. This BIST testing normal operation of the circuit, without need the set of the circuit condition. It is fully based on the concurrent BIST.Main advantages of the scheme is hardware overhead, error detection and concurrent test latency(CTL).Linear feedback shift register (LFSR) is existing system for the project.LFSR can't operate on offline operation time. In this proposed system, generate the test pattern generation on running time at the same time we checking the circuit unit. This proposed scheme is to perform better than the existing system

Keywords*:* Built-in self test (BIST), concurrent test latency (CTL), linear feedback shift register (LFSR).

1. INTRODUCTION

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT).The basic BIST architecture requires the addition of three hardware blocks to a digital circuit, a test pattern generator, a response analyzer, and a test controller. The test pattern generator generates the test patterns for the CUT.

A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compacts and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit. In normal operation, the CUT receives its inputs from other modules and performs the function for which it was designed.

During test mode, a test pattern generator circuit applies a sequence of test patterns to the CUT, and the test responses are evaluated by a output response compactor. In the most common type of BIST, test responses are compacted in output response compactor to form (fault) signatures. This is the fraction of faults of interest that can be exposed by the test patterns produced by pattern generator and detected by output response monitor This undesirable property is called masking or aliasing.

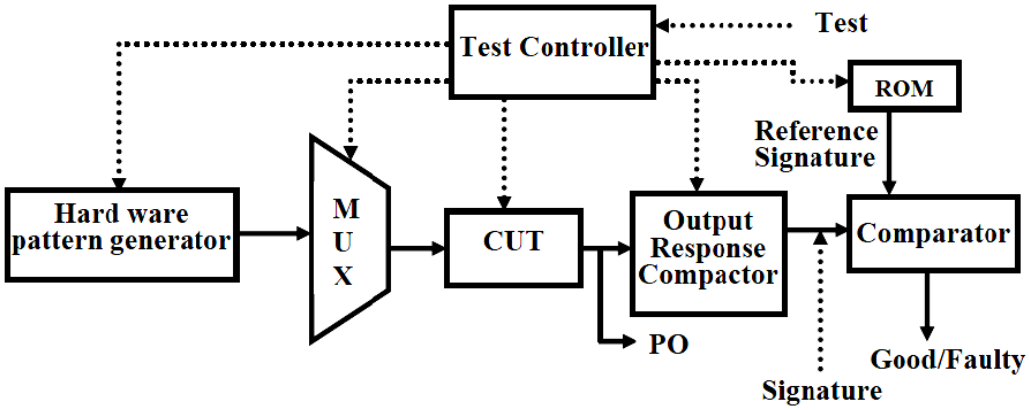

Figure 1: A Typical BIST Architecture

2. BIST TEST PATTERN GENERATION TECHNIQUES

2.1 Stored patterns

An automatic test pattern generation (ATPG) and fault simulation technique is used to generate the test patterns. A good test pattern set is stored in a ROM on the chip. When BIST is activated, test patterns are applied to the CUT and the responses are compared with the corresponding stored patterns. Although stored-pattern BIST can provide excellent fault coverage, it has limited applicability due to its high area overhead

2.2 Exhaustive patterns

Exhaustive pattern BIST eliminates the test generation process and has very high fault coverage. To test an n-input block of combinational logic, it applies all possible 2^n-input patterns to the block. Even with high clock speeds, the time required to apply the patterns may make exhaustive pattern BIST impractical for a circuit with n>2.

2.3 Pseudo-exhaustive patterns

In pseudo-exhaustive pattern generation, the circuit is partitioned into several smaller sub-circuits based on the output cones of influence, possibly overlapping blocks with fewer than *n* inputs. Then all possible test patterns are exhaustively applied to each sub-circuit. The main goal of pseudo-exhaustive test is to obtain the same fault coverage as the exhaustive testing and, at the same time, minimize the testing time. Since close to 100% fault coverage is guaranteed, there is no need for fault simulation for exhaustive testing and pseudo-exhaustive testing. However, such a method requires extra design effort to partition the circuits into pseudo-exhaustive testable sub-circuits. Moreover, the delivery of test patterns and test responses is also a major consideration. The added hardware may also increase the overhead and decrease the performance.

2.4 Pattern Generation by Counter

In a BIST pattern generator based on a folding counter, the properties of the folding counter are exploited to find the seeds needed to cover the given set of deterministic patterns. Width compression is combined with reseeding to reduce the hardware overhead. In a two-dimensional test data compression technique an LFSR and a folding counter are combined for scan-based BIST. LFSR reseeding is used to reduce the number of bits to be stored for each pattern (horizontal compression) and folding counter reseeding is used to reduce the number of patterns (vertical compression).

3. PROPOSED SYSTEM

Built-in self test (BIST) techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage, whereas simultaneously they relax the reliance on expensive external testing equipment. Hence, they constitute an attractive solution to the problem of testing VLSI devices. BIST
techniques are typically classified into offline and online. Offline architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV). Therefore, to perform the test, the normal operation of the CUT is stalled and, consequently, the performance of the system in which the circuit is included, is degraded.

Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation. These architectures test the CUT concurrently with its normal operation by exploiting input vectors appearing to the inputs of the CUT, if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig.3.1. The CUT has *n* inputs and *m* outputs and is tested exhaustively, hence, the test set size is $N = 2n$. The technique can operate in either normal or test mode, depending on the value of the signal labelled *T/N*.

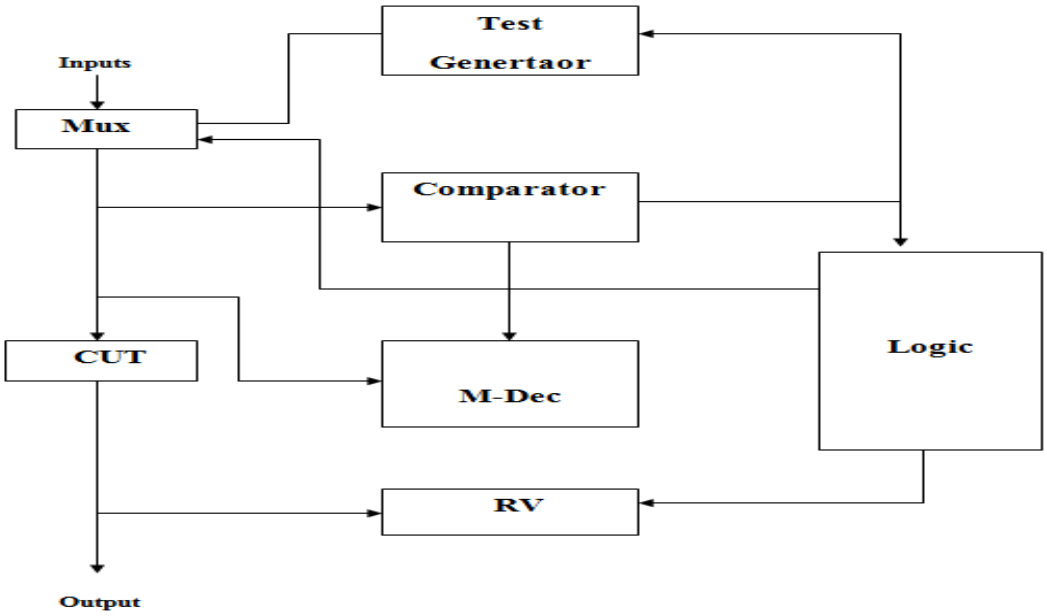

Figure 3.1: Proposed BIST Architecture

At the beginning of the operation, the module is reset through the external reset signal. When reset is issued, the tge signal is enabled and all the outputs of the decoder are enabled. Hence, DA1, DA2, ... , DA W are one. Furthermore, the CD signal is enabled therefore, a one is written to the right hand side of the cells and a zero value to the left hand side of the cells.

During normal mode, the inputs to the CUT are driven from the normal inputs. The n inputs are also driven to the CBU as follows: the w low-order inputs are driven to the inputs of the decoder, the k high-order inputs are driven to the inputs of the comparator. When a vector belonging to the current window reaches the inputs of the CUT, the comparator is enabled and one of the outputs of the decoder is enabled. During the first half of the clock cycle (clk and cmp are enabled) the addressed cell is read, because the read value is zero, the w-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During

the second half of the clock cycle, the left flip-flop (the one whose clock input is inverted) enables the AND gate (whose other input is clk and cmp), and enables the buffers to write the value one to the addressed cell.

If the cell corresponding to the incoming vector contains a one (i.e., the respective vector has reached the CUT inputs during the examination of the current window before), the rve signal is not enabled during the first half of the clock cycle; hence, the w-stage counter is not triggered and the AND gate is not enabled during the second half of the clock cycle.

When all the cells are full (value equal to one), then the value of the w-stage counter is all one. Hence, the activation of the rve signal causes the e counter to overflow, hence in the next clock cycle (through the unit flop delay) the tge signal is enabled and all the cells (because all the outputs of the decoder are enabled) are set to zero. When switching from normal to test mode, the w-stage counter is reset. During test mode, the w-bit output of the counter is applied to the CUT inputs. The outputs of the counter are also used to address a cell. If the cell was empty (reset), it will be filled (set) and the RV will be enabled. Otherwise, the cell remains full and the RV is not enabled.

4. CONCLUSION

Design of MDEC concurrent Built-in self test (BIST) designed for self testing process chip (or) circuit. This BIST testing normal operation of the circuit, without need the set of the circuit condition. It is fully based on the concurrent BIST.Main advantages of the scheme is hardware overhead, error detection and concurrent test latency(CTL).The proposed scheme ,generate the test pattern generate on circuit online mode, as well as checking the circuit unit. The proposed MDEC concurrent BIST scheme is to reduce the hardware overhead, CTL and errors.

REFERENCES

[1] Voyiatzis, T. Haniotakis, C. Efstathiou, and H. Antonopoulou, “A concurrent BIST architecture based on monitoring square windows,” in *Proc. 5th Int. Conf. DTIS*, Mar. 2010, pp. 1–6.

[2] .M. A. Kochte, C. Zoellin, and H.-J. Wunderlich, “Concurrent self-test with partially specified patterns for low test latency and overhead,” in *Proc. 14th Eur. Test Symp.*, May 2009, pp. 53–58.

[3] S. Almukhaizim and Y. Makris, “Concurrent error detection methods for asynchronous burst mode machines,” *IEEE Trans. Comput.*, vol. 56, no. 6, pp. 785–798, Jun. 2007.

[4] S. Almukhaizim, P. Drineas, and Y. Makris, “Entropy-driven parity tree selection for low-cost concurrent error detection,” *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 25, no. 8, pp. 1547–1554, Aug. 2006.

[5] J. Rajski and J. Tyszer, “Test responses compaction in accumulators with rotate carry adders,” *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 12, no. 4, pp. 531–539, Apr. 1993.

[6] I. Voyiatzis, “On reducing aliasing in accumulator-based compaction,” in *Proc. Int. Conf. DTIS*, Mar. 2008, pp. 1–12.

[7] L. R. Huang, J. Y. Jou, and S. Y. Kuo, “Gauss-eliminationbased generation of multiple seed-polynomial pairs for LFSR,” *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 16, no. 9, pp. 1015–1024, Sep. 1997.

[8] Y. Zorian and A. Ivanov, “An effective BIST scheme for ROM’s,” *IEEE Trans. Comput.*, vol. 41, no. 5, pp. 646–653, May 1992.