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DESIGN OF SIX TRANSISTOR FULL ADDER CELL FOR VLSI APPLICATIONS

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Abstract—This paper presents a new design of 2T XNOR circuit. A six transistor full adder has been designed using the proposed 2T XNOR circuit. The circuit shows power consumption variation in the range of 125.1241µW to 421.7256 µW. Maximum output delay of the circuit shows variation in the range of 4.2528 ns to 3.1605 ns. Also, power-delay product (PDP) of circuit is changing from 532.1277 (fJ) to 1332.8637 (fJ) with alteration in supply voltage from 1.8V to 3.3V. The designed 6T full adder has been compared with earlier reported full adder circuits and a considerable improvement in power consumption, PDP and area has been obtained. The simulation has been carried using SPICE in TSMC 0.18µm CMOS technology.

Keywords:- 2T (two transistor); CMOS; delay; full adder; low power; transmission gate (TG)

1. INTRODUCTION

With the increasing demand of low power integrated circuits for portable equipment's like PDA, laptops, mobile phones etc., design selections which take into pertain of low power features. Low power applications have become known as a field of primary concern for VLSI (very large scale integration) system designers. Power reduction is one of the main concerns in today VLSI design style because of the long battery operating life condition of portable devices and due to growing number of transistors on a single chip leads to high power consumption [1]. The VLSI circuit's power consumption can be split into three important components: static (or leakage), dynamic and short circuit power consumption [2].

$$P_{total} = P_{dynamic} + P_{short\ circuit} + P_{leakage} \quad (1)$$

The static power consumption is due to unwanted sub threshold current in the transistor channel when the transistor is turned off. The dynamic power dissipation is also called the switching power dissipation is the charging or discharging of the nodal capacitances during a low to high or high to low transition at the output node. The square of the input supply voltage is proportional to the dynamic power dissipation. The short circuit power consumption occurs during the transistor switching because current flowing from power supply to ground [11], [14].

Addition is the most commonly used arithmetic operation in various VLSI systems. Adders are the essential elements in microprocessors, data processing units, digital signal processors (DSP), ALUs, compressors and so on. The multiplication and division circuits have the full adder in their critical paths and thus influence the overall circuit performance [4]. The critical path dwells of transistors that generate the highest delay in the output signal.

Therefore, a full adder becomes crucial building blocks in VLSI systems and efficient implementation of full adder improves the circuit performance [6], [9]. The conventional CMOS 28T full adder design with pull up and pull down network presents good driving capability and high noise margin [3]. The main disadvantage of conventional CMOS 28T full adder use of large number of transistors results in high power consumption and more area. A [7] full adder circuit based on hybrid pass logic using 22 transistors has been presented in which pass logic style has been used to efficiently produce the XOR and XNOR outputs simultaneously. CMOS transmission gate adder (TGA) using 20 transistors is report in [10]. Main disadvantage of this adder is that it needs double transistors than that of pass transistor logic for implementations of same logic function. The power consumption of this circuit is more than the 28T adder. The static energy recovery full adder circuit (SERF) utilize just 10 transistors has been presented [5]. It has low power dissipation but it cannot be cascaded at low power supply because of various threshold problems. In the 8 transistors full adder design, one inverter and three multiplexers are used to minimize the power consumption and transistor count [8]. In this paper, a new design of XNOR circuit has been proposed using two NMOS transistors and three resistances. Based on the proposed XNOR circuit a six transistors full adder has been designed. The rest of paper is structured as follows: Section II introduce the new design of two transistors XNOR circuit and a single bit full adder based on XNOR circuit and multiplexer has been implemented. In section III simulation results of proposed full adder are discussed and compared with preceding adder circuits. Finally section IV drawn the conclusions.

1. FULL ADDER CIRCUIT DESCRIPTION

A single bit full adder has three inputs A, B, C and produce two outputs of single bit SUM and COUT. The single bit full adder functionality is based on the following equations:

$$SUM = (A \oplus B) \oplus C \quad (2)$$

$$COUT = A \bullet B + C \bullet (A \oplus B) \quad (3)$$

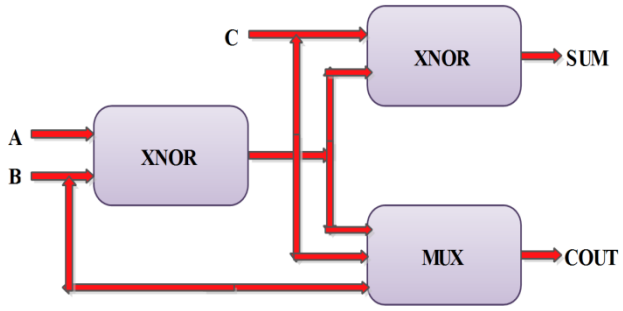


Fig. 1(a): Block diagram of full adder

A	B	C	SUM	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Truth table for full adder

Standard approach as shown in figure 1 for implementation full adder using XOR and XNOR has been generally used [15]. The XOR and XNOR circuits are primal building blocks in numerous circuit particularly full adders and multipliers. The arithmetic circuit's performance is influence by the individual performance of the XOR and XNOR circuits that are incorporated in them [16]. Hence, attentive analysis and design is compulsory for XOR and XNOR circuits to get full output voltage. Furthermore, the design should have a lesser number of transistors to implement XOR-XNOR circuits for smaller power dissipation.

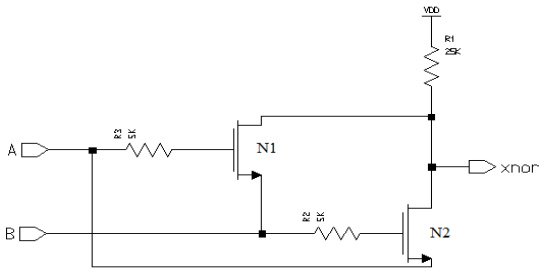


Fig. 2: (a) Design of proposed XNOR circuit

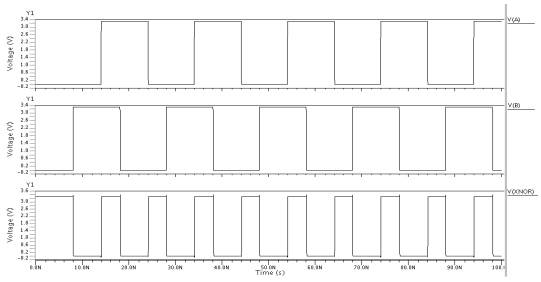


Fig. 2: (b) Output waveform of XNOR circuit

The proposed XNOR circuit with two NMOS transistors has been exhibited in figure 2(a). When both inputs 'A' and 'B' are low then NMOS transistor (N1) and (N2) are off and provide high logic at output. With input combination 'A' is high and 'B' is low, N1 is on, while N2 is off and low logic at output. High logic at the output with inputs 'A' and 'B' are high because both transistors are turned on. In final case for input 'A' is low and 'B' is high. In this condition, transistor N1 is off and N2 is on. This shows low logic at output. So the proposed circuit displays full swing operation for all input combinations as XNOR gate. Figure 2(b) shows the output waveform of the proposed XNOR circuit. The proposed full adder circuit has been created by joining all the designed components as shown in figure 1(a). It incorporates two XNOR gates and a single 2 to 1 multiplexer circuit**.** Sum is generated by two XNOR gates and cout is generated by two transistors multiplexer block. It prove the improved performance than the previous reported full adder circuits and obtain less area due to less numbers of transistors. The single bit full adder using proposed XNOR gate with six transistors has been implemented and shown in figure 3**.**

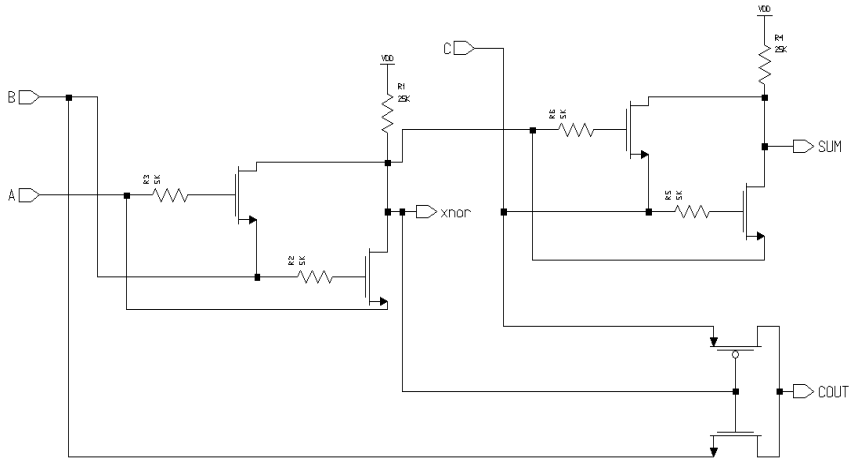


Fig. 3: Proposed six transistors full adder circuit

2. SIMULATION RESULTS AND DISCUSSION

The simulation has been carried out with supply voltage ranging from [1.8-3.3] V, which permit us to compare the power consumption, delay, PDP (power delay product) and EDP (energy delay product) of the proposed full adder circuit. The simulation results of the proposed circuit have been compared with the previous reported CMOS full adder circuits. All the circuits has been simulated and designed in 0.18µm CMOS process.

Table 1: Power, delay, PDP and EDP of proposed full adder circuit

Supply voltage (V)	Power consumption (μW)	Maximum output delay (ns)	PDP (fJ)	EDP $\times 10^{-24}$(J)
1.8	125.1241	4.2528	532.1277	2263.0326
2.0	154.7413	3.8566	596.7752	2301.5232
2.3	204.9364	3.7545	769.4337	2888.8388
2.5	242.2366	3.5672	864.1063	3082.4399
2.7	282.5968	3.4280	968.7418	3320.8468
3.0	348.8581	3.2241	1124.7534	3626.3174
3.3	421.7256	3.1605	1332.8637	4212.5157

Table 1 shows the power consumption, delay, PDP and EDP with varying supply voltage from 1.8V to 3.3V for the proposed full adder circuit. Power consumption varies from 125.1241 μW to 421.7256 μW with variation of supply voltage from 1.8V to 3.3V. Maximum output delay shows variations from 4.2528 ns to 3.1605 ns and power delay product (PDP) of full adder 532.1277 (fJ) to 1332.8637 (fJ) respectively. Further, energy delay product (EDP) varies from 2263.0326×10^{-24} (J) to 4212.5157×10^{-24} (J) with variation of supply voltage from 1.8V to 3.3V. Simulation input and output waveforms of proposed full adder circuit shown in figure 4.

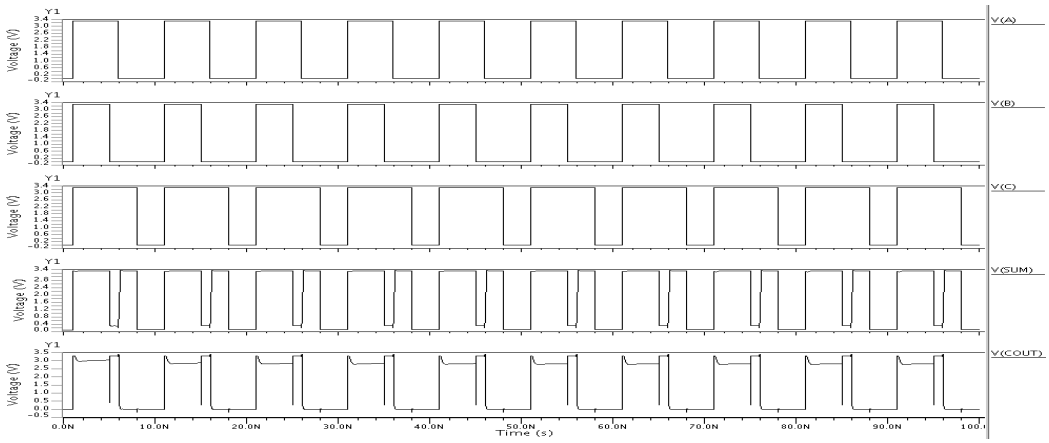
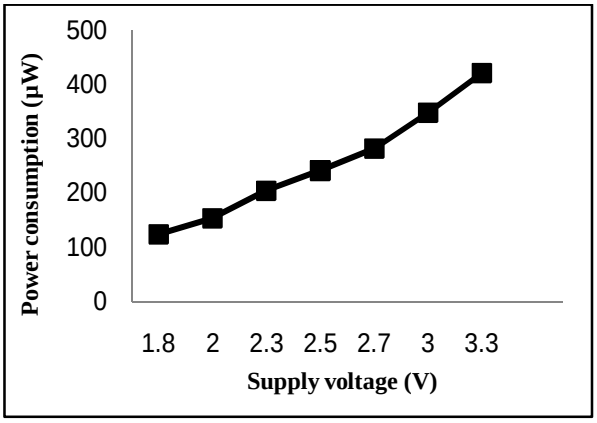
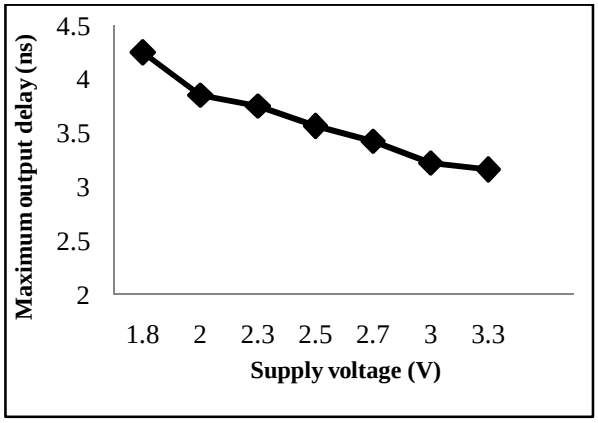


Fig. 4: Simulation input and output waveform of proposed full adder circuit





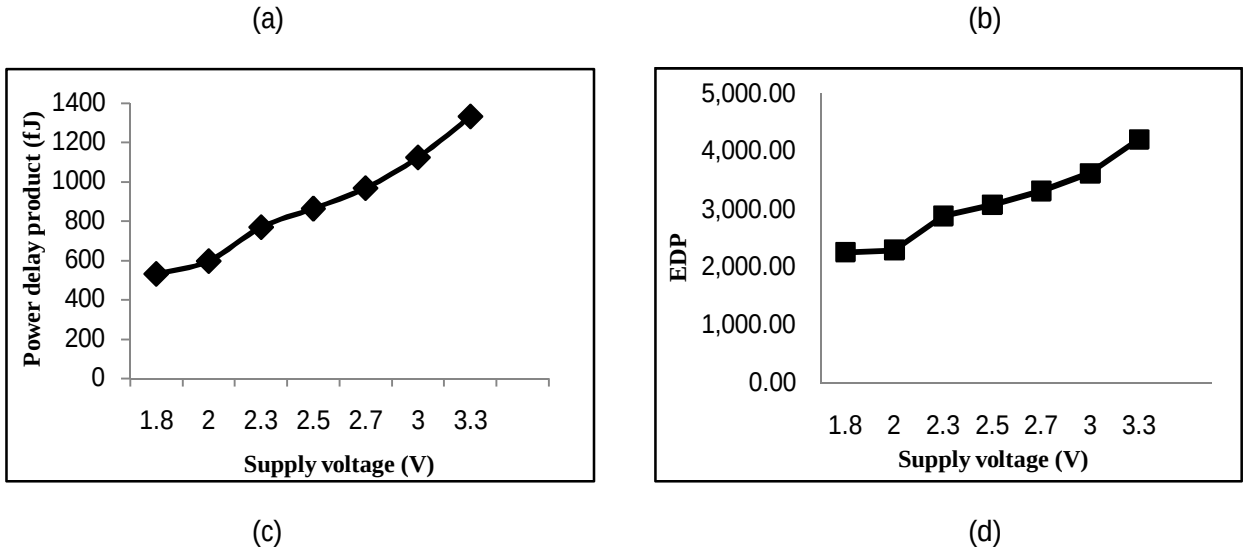


Fig. 5: (a) Power consumption (b) Output delay (c) PDP (d) EDP of full adder circuits versus supply voltage

Figure 5(a) shows the power consumption of full adder circuit with variation in supply voltage. From this, it has been observed that power consumption of adder circuit is increasing with increase in supply voltage. Figure 5(b) shows the maximum output delay variation of adder circuit, delay decrease with rise in supply voltage. The power delay product (PDP) variation shown in figure 5(c). The PDP compromise between speed and power consumption and is a quantitative determine of the efficiency. PDP and EDP are mainly significant when high speed and low power process is mandatory. Moreover, figure 5(d) demonstrates the energy delay product variation of full adder circuit. According to table 3, even through proposed circuit has six transistors, it still show less power dissipation.

Table 2: Comparison between different types of full adder designs

Full adder type	Power consumption (µW)	Number of transistors for design
Conventional [3]	946.1168	28
22T adder [7]	546.2890	22
TG adder [10]	371.6328	20
10T SERF [5]	263.0386	10
8T adder [8]	197.1043	8
This work	125.1241	6

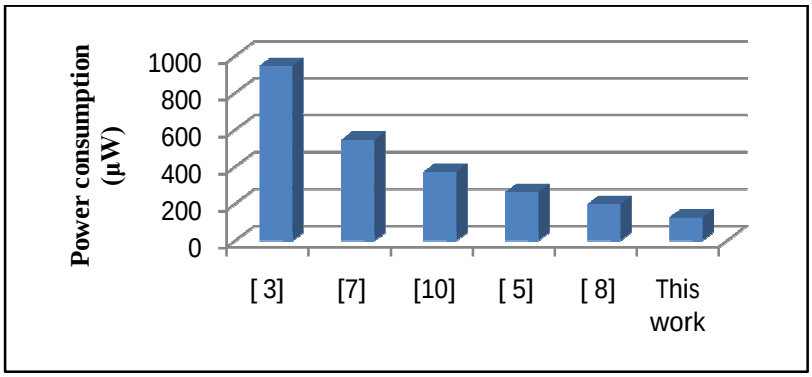


Fig. 6: Power consumption comparison of full adder cells

3. CONCLUSIONS

In this paper a power and area efficient design of a single bit full adder has been introduced. The characteristics of the proposed full adder circuit are compared against earlier reported full adder circuits based on the power consumption. The proposed full adder shows power consumption of 125.1241µW and maximum output delay of 4.2528 ns. Further, circuit shows PDP of 532.1277 (fJ) and EDP of 2263.0326× 10^{-24}(J) with supply voltage of 1.8V. The analysis of simulation results proven that the performances of the newly proposed full adder circuit is superior in terms of power consumption and delay due to less number of transistors. All the results are simulated using 0.18µm CMOS process.

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