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HIGHER ORDER IMPLEMENTATION OF SQUARER AND CUBE USING VEDIC SUTRAS

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Abstract: The paper proposes higher order square and cube architectures that play a major role in Digital design used in real time applications. These architectures are useful for higher order computations by using the Vedic sutras. By using the Dwandwa yoga duplex combination properties of Urdhva Tiryagbhyam sutra of Vedic mathematics. The Proposed designs prove efficient for high speed and low power applications like in Arithmetic and Logic Unit replacing the traditional architectures. The results are evaluated in terms of delay, area and power consumption for the device Spartan3E - XC3S500E-5FG320 using Xilinx ISE 10.1i Tools.

Key Words: Vedic mathematics, Dwandwayoga method.

1. Introduction

Power of a number is a improved version of multiplication used in thrust areas of Engineering and Technology like DSP applications. This is achieved using Vedic square and cube architecture. Power, area and speed (delay) of circuit gives the performance of the circuit. For multiplication, criss cross method of 'Urdhva Tiryagbhyam" and other methods include Vedic multipliers based on 'Urdhva Tiryagbhyam' and the "Duplex" properties of 'Urdhva Tiryagbhyam'. Therefore, the main motivation behind this work is to investigate the VLSI Design and Implementation of powering Circuit architecture with reduced delay.

2. Vedic Mathematics:

Vedic Mathematics (VM) is an ancient system of mathematics that was re-discovered by Sri Bharati Krishna Tirthaji between 1911 and 1918. Tirthaji (1884-1960) was an Indian scholar well versed in the areas of Sanskrit, English ,Mathematics, Astronomy and many other areas of science .He deciphered ancient Indian texts, known as the "Ganitasutras", (which means mathematics) to discover 16 short verses, known as "Sutras". These sutras, when applied correctly, will enable the user to solve many types of mathematics problems mentally without having to use pencil and paper in a fraction of the time in would take otherwise. Tirthaji wrote sixteen books, one for each sutra, describing the application of each to the solution of math problems .Unfortunately, these books were lost. Tirthaji attempted tore-write all of these books from memory, but was only able to complete the first volume entitled "Vedic Mathematics" before his death. This book, which is available today, is the seminal work on Vedic Mathematics.

Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Sankaracharya of Puri culled a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He developed methods and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics. According to him, there has been considerable literature on Mathematics in the Veda- sakhas. Unfortunately most of it has been lost to humanity as of now. This is evident from the fact that while, by the time of Patanjali, about 25 centuries ago, 1131 Veda-sakhas were known to the Vedic scholars, only about ten Veda-sakhas are presently in the knowledge of the Vedic scholars in the country. The Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Application of the Sutras saves a lot of time and effort in solving the problems, compared to the formal methods presently in vogue]. Though the solutions appear like magic, the application of the Sutras is perfectly logical and rational. The computation made on the computers follows, in a way, the principles underlying the Sutras. The Sutras provide not only methods of calculation, but also ways of thinking for their application. The following are the Vedic sutras and their meaning.

1. Ekadhikena Purvena: One more than the previous
2. Nikhilam Navatascharamam Dastah: All from nine and last from ten
3. Urdhwa-tiryagbhyam: Criss-cross
4. Sunyam Samyasamuchchaye: When the samuchchaya is the same, the samuchchaya is zero, and i.e. it should be equated to zero.
5. (Anurupye) Sunyamanyat: If one is in ratio, the other one is zero.
6. Sankalana-vyavkalanabhyam: By addition and by subtraction
7. Puranpuranabhyam: By completion or non-completion
8. Chalana-Kalanabhyam: Differential
9. Yavdunam: Double
10. Vyastisamastih: Use the average
11. Sesanyankena Charmena: The remainders by the last digit
12. Sopantyadyaymantyam: The ultimate & twice the penultimate
13. Ekanyunena Purven: One less than the previous
14. Gunitasamuchachayah: The product of the sum of coefficients in the factors
15. Gunaksamuchchayah: When a quadratic expression is product of the binomials then its first differential is sum of the two factors.
16. Paravartya Yojajet: Transpose and adjust.

In order to find the power of a number is performed by using the square of a binary number. Square can be calculated using “Duplex” property of Urdhava Tiryagbhyam .Duplex of a number is twice the product of the outer most pair, till no other pairs to be left .if there are odd number of bits then one bit left alone and take square of that bit. Thus for the number 95673, then D=2* (9*3) +2*(5*7) +6*6=160.

Then , Duplex can be given as follows

For a 1 bit number D is its square.

For a 2 bit number D is twice their product.

Thus D (1) =1*1;
D (11) =2*1*1;
D (101) =2*1*1+0*0;
D (1011) =2*1*1+2*0*1;

Here multiplying with 2 denotes shifting left side by one bit.

3. Implementation of Higher order powers using square and cube architecture:

Higher order powers is nothing but implementation power of 4,5 etc., In Vedic mathematics for squaring Ekadhikena Purvena sutra used to square that are ending with 5 only. Yavadunam sutra used to find the square near to base 10,100,1000 etc., hence to find the square of any number using Duplex method of Urdhava Tiryagbhyam .square of number calculated by two different ways(a^2 ,b^2,2ab).the first two by the duplex and third one using the criss- cross multiplication.

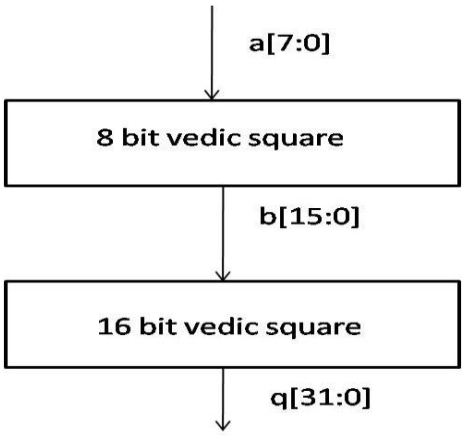

Fig: 1.Power four of number (a^4)

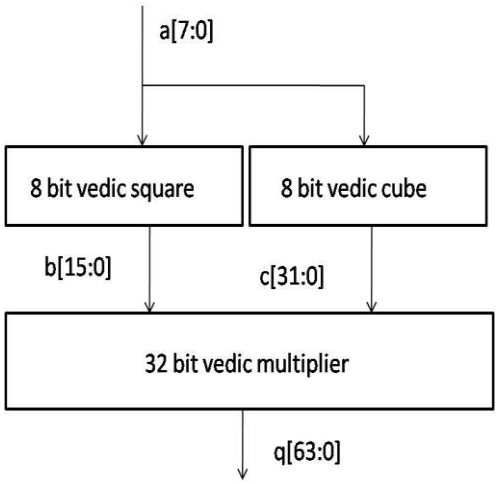

Fig: 2. Power five of number (a^5)

Power of four can be calculated by using two square architectures .one is 8-bit and other 16-bit square architecture. firstly the 8-bit number divided in to two parts each of 4-bit and find the square for two parts using duplex property and multiply twice of first and second one .and add them up making sure not to carry over excess digits from left to right as given in the fig. after getting the 8-bit output then perform the 16-bit square operation to get the final answer .In order to implement 16-bit square replace 4-bit with 8-bit Vedic multiplier and in place of 4-bit square use 8-bit square and add them from left to right.

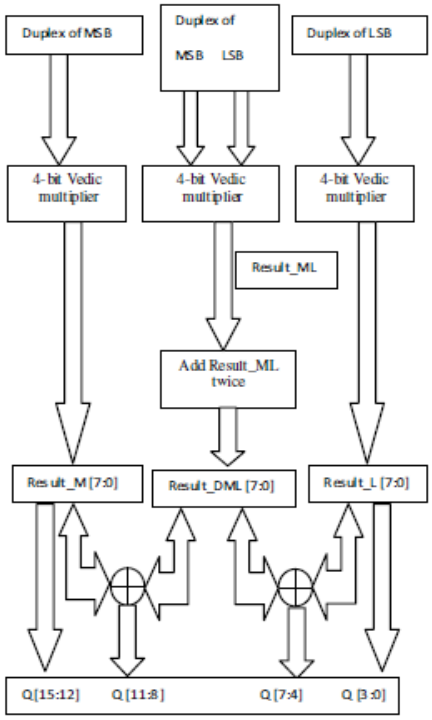

Fig:3. 8-bit square architecture

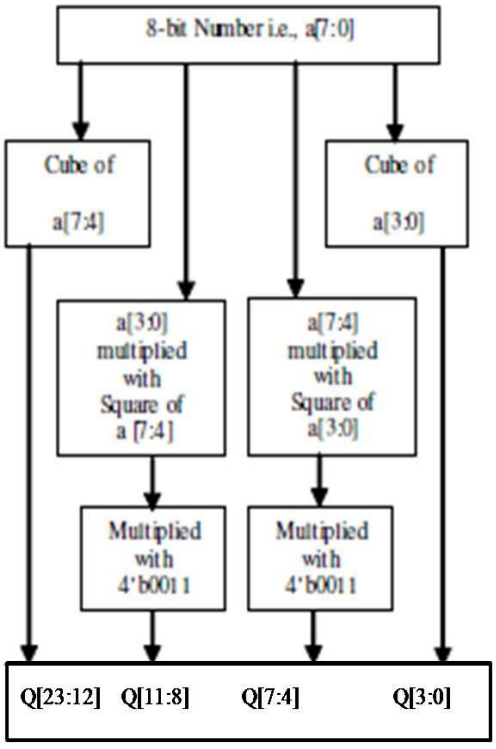

fig:4. 8-bit cube architecture

Power of five can calculated using with square, cube and Vedic multiplier architecture. Cube calculated individually a^3, a^2b,ab^2, b^3 and then multiply with 3 of terms a^2b,ab^2 and add them from to right without carry cross-over bits .after that multiply with 32-bit Vedic conventional multiplier to get required answer.

4. Results:

In this paper 8-bit higher order powers architectures are implemented using Verilog HDL. Logic synthesis is implemented using Xilinx ISE simulator and compared with the conventional method. The simulation results and comparison table these are well used in the computer hardware design.

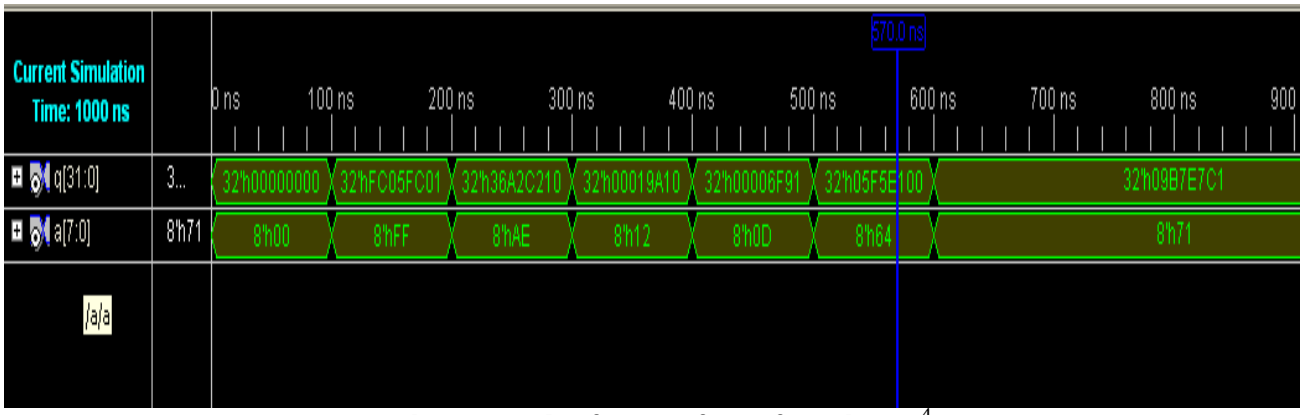

Fig5: Simulation result of power four of number (a^4)

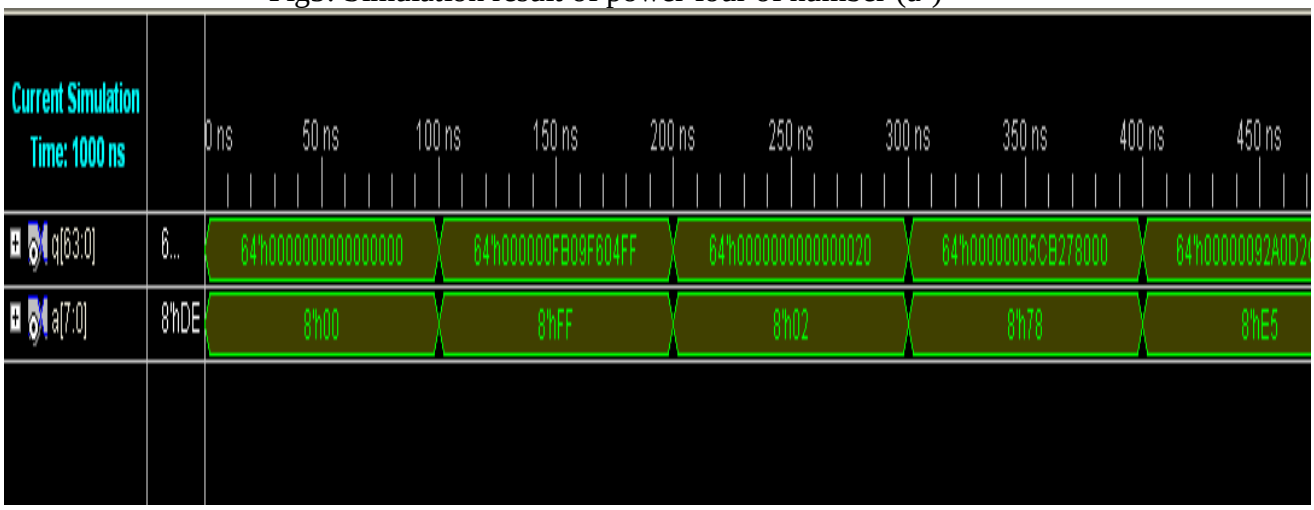

Figure6: Simulation result of power five of number (a^5)

	Power(mw)	Speed(ns)
Vedic	133	24
conventional	155	30

Table 1: comparison of power 4 of a number

	Power(mw)	Speed(ns)
Vedic	148	30
conventional	165	37

Table 2: comparison of power 5 of a number

In the simulation of power four of a number we get the output as 19A10 for the input of 12 with power dissipation of 133 mw and speed(delay) of 24 ns .similarly the simulation of power five of a number we the output as 20 for in input of 2. With power dissipation of 148 mw and speed (delay) of 37ns.

Conclusion:

In this paper we have represented the implementation of higher order powers using squarer and cube architecture using Vedic mathematics. Due to Vedic methods it is faster than conventional methods. Due to factors of low speed, low power higher order powers implemented in arithmetic and logical units and polynomial and algebraic equations by replacing the regular methods. Similarly for number of bit size can be implemented for 16,24 etc. For example, implementation of squaring of 24 bits implemented by 32 –bit square with the assumption of 8 MSBs as zero. The design is implemented using Xilinux10.1i tool for XC3S500E-5FG320. The idea proposed here may set path for future research in this direction. Future scope of research is to reduce area requirements.

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