LOW POWER DOUBLE EDGE PULSE TRIGGERED FLIP FLOP DESIGN

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Abstract

In this paper a novel low power double edge pulse triggered flip flop (FF) design is present. First, the pulse generation control logic by using the NAND function and is removed from the critical path to facilitate a faster discharge operation. A simple two transistor NAND gate design is used to reduce the circuit complexity. Second, a double edge conditional discharging flip flop is used to reduce the switching activity and also the different techniques are there to reduce. As a result, transistor sizes in delay inverter and pulse-generator circuit can be reduced for power saving, Various simulation results based on CMOS 90-nm technology reveal that the Double edge modified hybrid latch flip flop design features the best power-delay-product performance in several FF design under comparison. Its maximum power saving design is up to 38.4%. Compared with the conversional transmission gate based flip flop design.

Keywords: Flip flop, low power, double edge, and pulse triggered flip flop.

1. Introduction

Flip flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital design now-a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design.

Pulse-Trigged (P-FF), Because of its single latch structure, is more popular than the conventional transmission gate (TG) and master-slave based FFs in high-seep applications besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A p-ff consisting of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-Triggered Flip Flop. Since only one latch, as opposed to two in the conventional master-slave configuration is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. A statistical design frame work is developed to take these factors into account. To obtain the balanced performance among power, delay, and area, design space exploration is also a widely used technique.

In this brief, we present a novel low power double edge P-FF design based on a signal feed through. Observing the delay discrepancy in latching data "1" and "0", the design manages to shorten the longer delay by

feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implementing by introducing a simple pas transistor for extra signal driving.

2. Double edge Pulse Triggered Flip flop

Flip-Flops and latches are clocked storage elements, which store values applied to their inputs. They are classed according to their behaviour during the clock phases. A latch is level sensitive. It is transparent and propagates its input to the output during one clock phase (clock low or high), while holding its value during the other clock phase. A Flip-Flop is edge triggered. It captures its input and propagates it to the output at a clock edge (rising or falling), while keeps the output constant at any other time. The design of this clocked storage an element is highly depended on the clocking strategy and circuit topology. This research focuses on synchronous system with edge-triggered clocking strategy, only Flip-Flop is discussed. In particular, double edge-triggered Flip-Flops are introduced and explored. Storage element generally stores its value as charges on a capacitor. CMOS Flip-Flop can be static or dynamic, depending on how it retains its values against charge leakage. A static Flip-Flop retains its value using positive feedback, while a dynamic Flip-Flop requires periodic refreshment of charges. Besides the method of retaining storage value, Flip-Flops are also classed by their topologies. Three types will be briefly discussed in the following: master-slave Flip-Flops, pulsed- based Flip-Flops, and amplifier-based Flip-Flops. Master-slave Flip-Flop is the most commonly used Flip-Flop topology in low power applications. It is composed of a master latch cascaded with a slave latch. These two latches are active during opposite clock phases. Pulsed-based Flip-Flop is popular for its soft-clock edge property, which allows time borrowing and alleviates clock skew penalty just like level-sensitive latch. It also provides superior latency and is capable of incorporating complex logic. Explicit type triggered flip flop and modified hybrid latch flip flop are the two examples of pulse based flip-flop. Amplifier-based Flip-Flop is mainly designed as a de-skewing element. Sense amplifier- based Flip-Flop (SAFF) is an example of amplifier-based Flip-Flop. It incorporates a precharged sense amplifier in the First stage to generate a negative pulse, and a set-reset (SR) latch in the second stage to capture and hold the results. But here we only discuss about pulse triggered flip flop.

2.1 Different Double edge Pulse triggered Flip Flops:

Pulse triggered flip flop in terms of pulse generator, can be classified as an implicit and explicit type. In an implicit type P-FF, The pulse generator is a part of latch design and no explicit pulse signals are to be generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit types P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an *n*-bit register). In this brief, we will thus focus on the explicit type P-FF designs only. Fig. 1(a) shows a classic Double edge explicit P-FF design, named data-close to- output (de ep-DCO) [7]. It contains a NAND-logic-based pulse generator. In this Double edge P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as Double edge conditional capture, Double edge conditional precharge, Double edge conditional discharge, and Double edge conditional pulse enhancement scheme have been proposed. But here only discussed about Double edge Conditional discharging Flip Flop. Fig. 2(a) shows a Double edge conditional discharged (CD) technique. An extra NMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up PMOS transistor only. Fig. 3(a) shows a similar P-FF design (DE SCDFF) using a Double edge static conditional discharge technique. It differs from the DECDFF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The Double edge modified hybrid latch flip flop (DEMHLFF) shown in Fig. 4(a) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the DEMHLFF design encounters two drawbacks. First, since node X is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse

(deviated by one VT*)* is applied to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra dc power.

2.2 Tools used:

- DSCH (Digital Schematic)
- Micro Wind

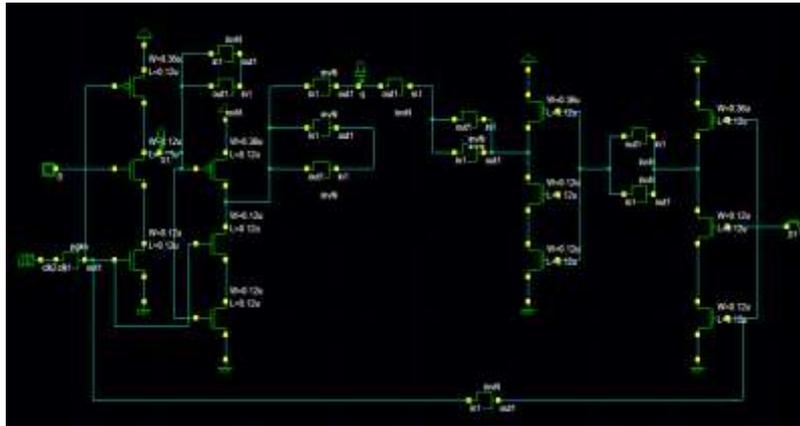## 3. Circuit Diagrams, Wave forms and Layouts for different DEP-FF:

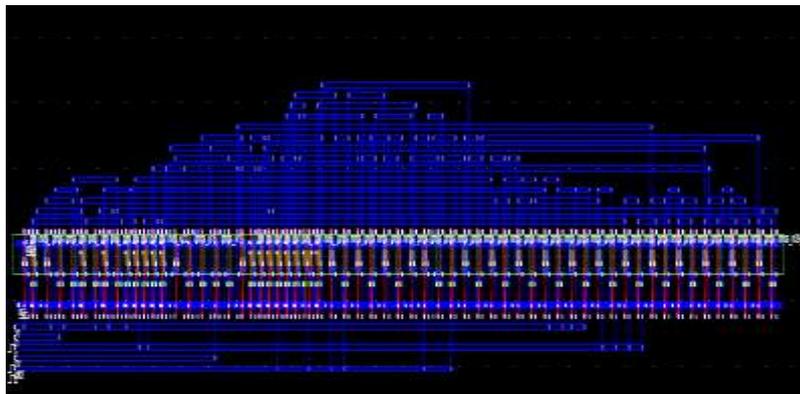Figure1," (A)" Double edge explicit-Data close to output
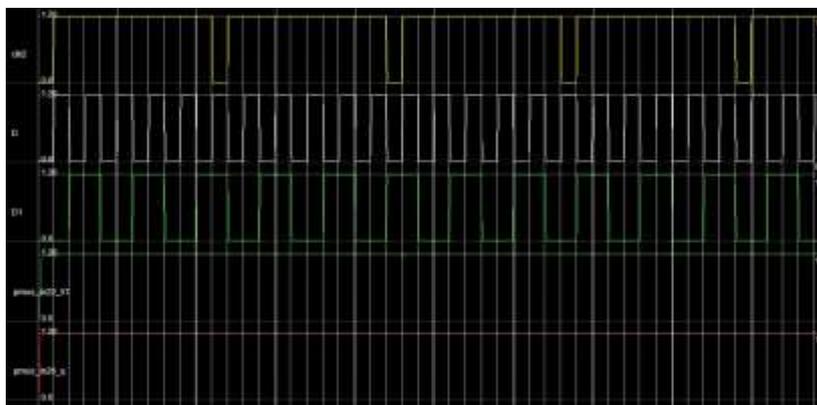

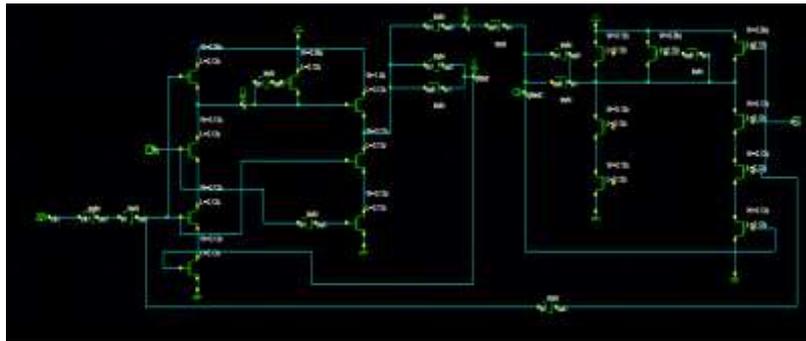Figure1," (B) Layout of DE EP-DCO

Figure1," (C)" Wave form of DEEp-DCO

Fig2," (A)" Double edge conditional discharging flip flop
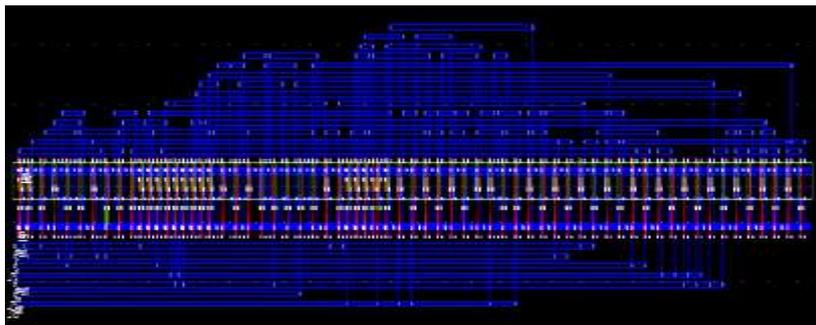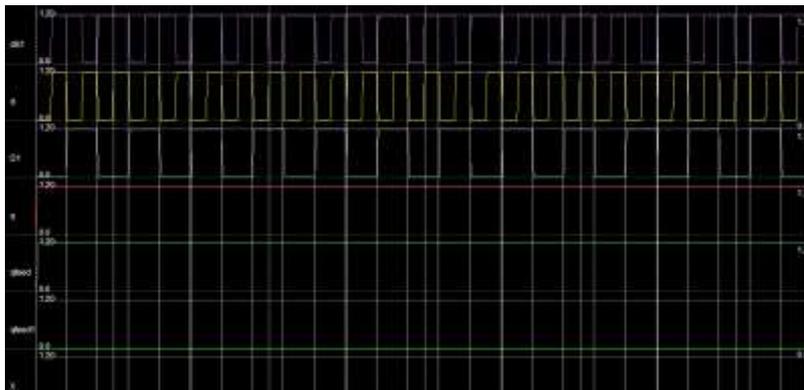

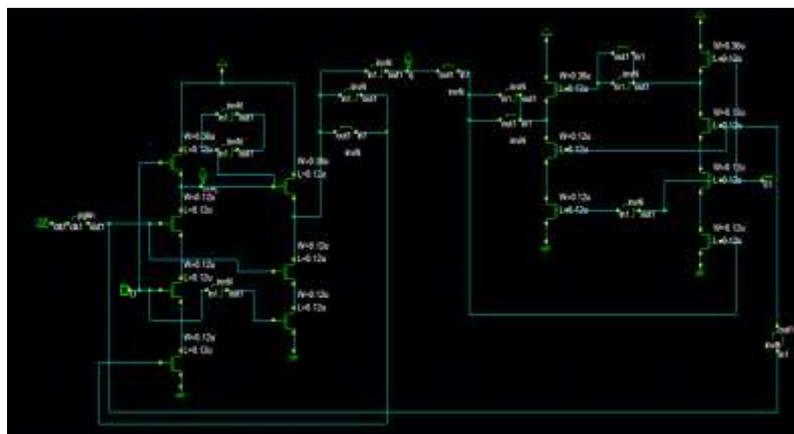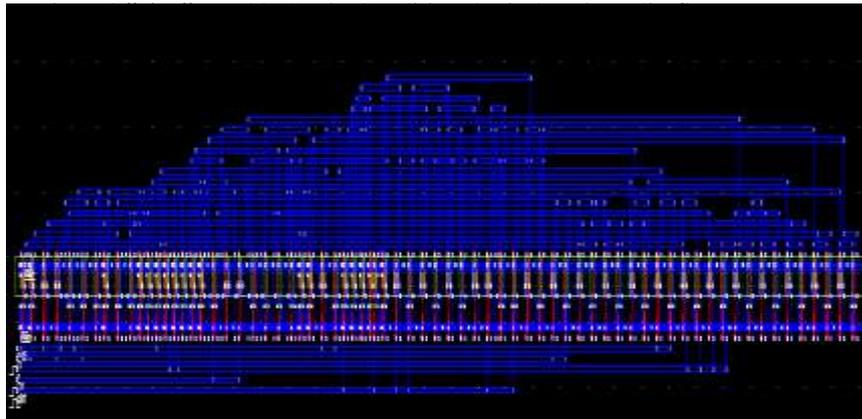Fig2," (B)" Layout of DE CDFF
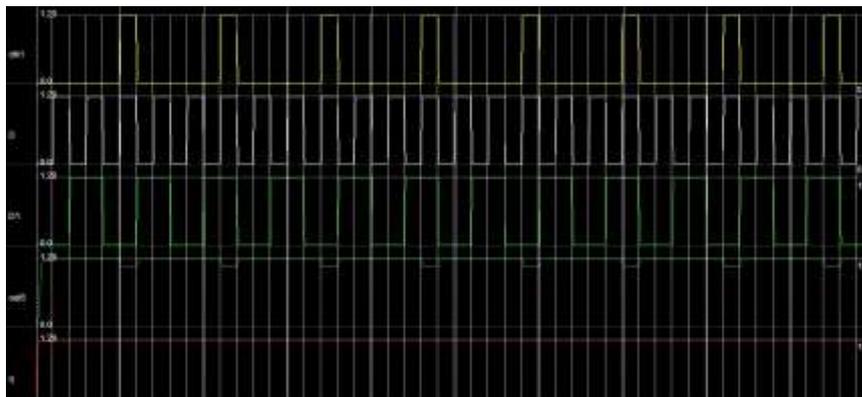

Figure2," (C)" Wave form of CDFF

Figure3,'' (B)'' Layout of SCDFF

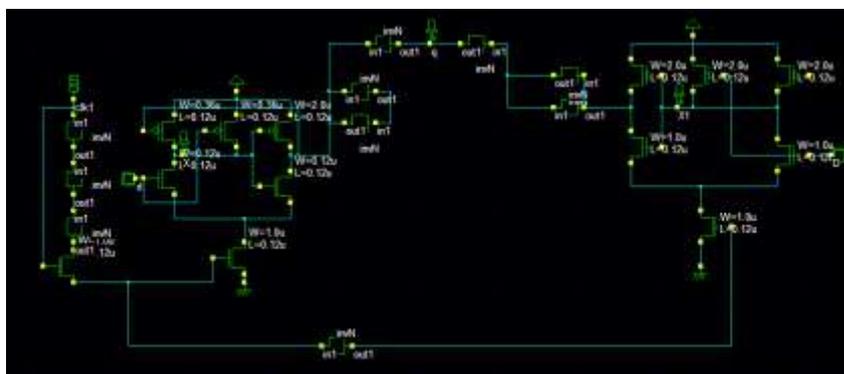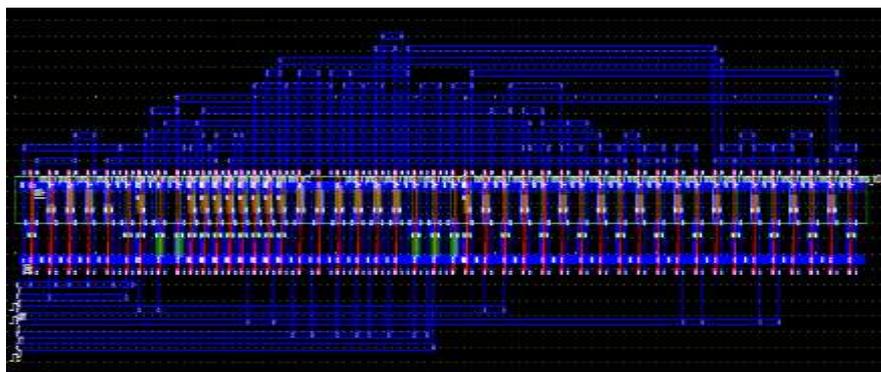Figure3,'' (C)'' Wave form of SCDFF

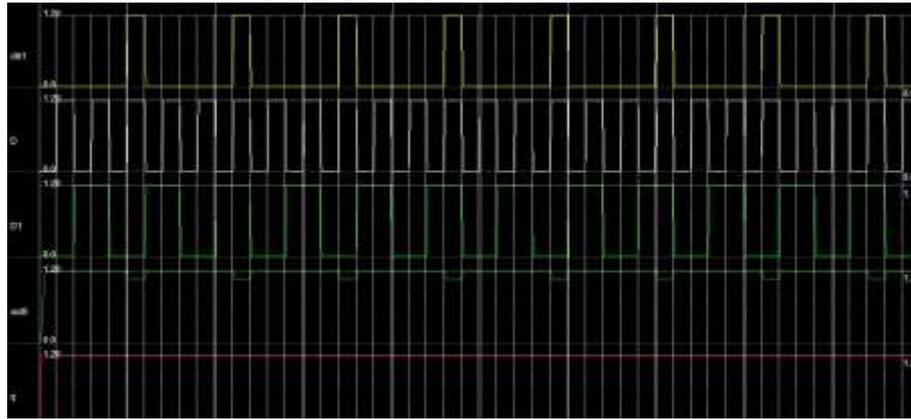Figure4,'' (A)'' Double edge Modified Hybrid Latch Flip flop

Figure4," (C)" Wave form of MHLFF

3.2 Tables

*Table1. Comparison of various Double edge Pulse triggered Flip flop design*

FF design	DE EP-DCO	DE CDFF	DE SCDFF	DE MHLFF
No of transistors	48	52	52	33
Layout area(μm^2)	1097.7	1259.1	1372.1	782.9
Setup Time(ps)	0.025	0.025	0.025	0.025
Hold Time(ps)	0.025	0.025	0.025	0.025
Average power (100%activity)μw	24.8	43.7	115.2	48.2
Average power (50%activity)μw	14.8	15.7	8.3	46.3
Average power (25%activity)μw	2.71	6.51	7.4	44.1
Average power (12.5%activity)μw	2.5	6.5	7.4	40.2
Average power (0% all-1)μw	15.5	6.3	7.1	46.2
Average power (0% all-0)μw	2.71	6.5	6.9	2.25
Power Dissipation μw	112.3	31.6	19.5	48.3

Table2: Leakage Power comparison in standby mode

FF Design	DE Ep-DCO	DE CDFF	DE SCDFF	DE MHLFF
(Clk,Data)=(0,0)	2.71	31.6	3.2	2.29
(Clk,Data)=(0,1)	2.8	2.51	2.9	2.2
(Clk,Data)=(1,0)	2.5	2.4	1.89	1.69
(Clk,Data)=(1,1)	1.9	2.3	1.8	0.69
Average	2.4	9.7	2.4	1.71

3.3 Graphs by Comparing power for different double edge triggered flip flop:
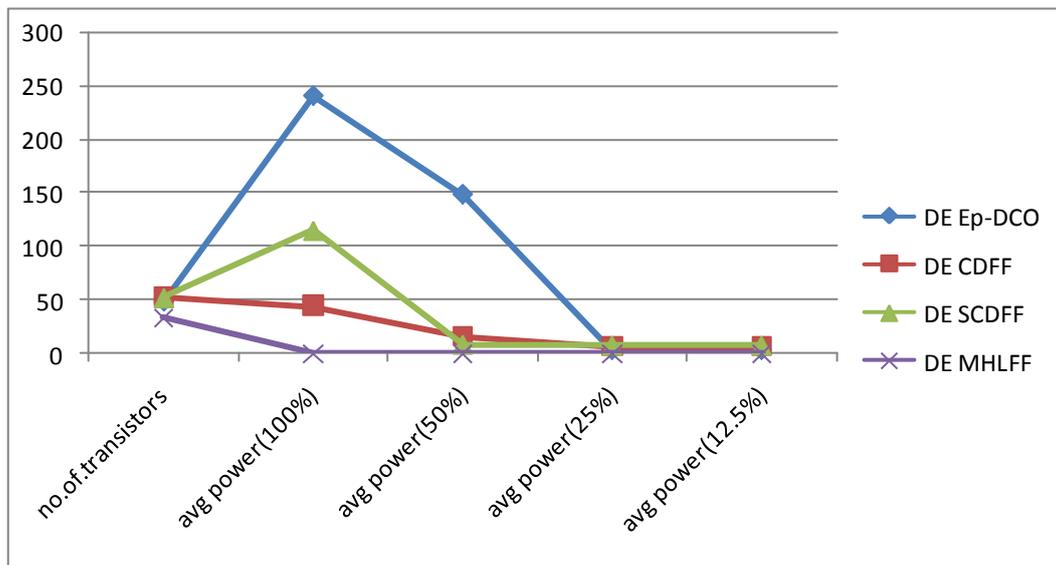
4. Conclusion

In this brief, we presented a novel P-FF design by employing a Double edge pulse triggered flip flop structure incorporating a mixed design style consisting of pass transistor and pseudo-NMOS logic. The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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A Brief Author Biography

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