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A CMOS BANDGAP AND SUB-BANDGAP VOLTAGE REFERENCE CIRCUITS FOR NANOWATT POWER LSIs

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Abstract

In this paper, an efficient bandgap reference (BGR) and sub-BGR circuits for Nano watt LSIs is presented. The circuits consist of a Nano-ampere current reference circuit, a bipolar transistor, and proportional-to-absolute-temperature (PTAT) voltage generators. The proposed circuits avoid the use of resistors and contain only MOSFETs and one bipolar transistor. The sub-BGR circuit divides the output voltage of the bipolar transistor without resistors, so that it can operate at a sub-1-V supply. The power dissipations are extremely low for the BGR and sub-BGR circuits. Sub- BGR circuit provides extremely very low power dissipation when compared to BGR circuits. It was implemented in Tanner EDA tool.

Keywords: Bandgap reference (BGR) circuits, CMOS analog integrated circuits, low- voltage, Nano watt, reference circuits

1. Introduction

The power supply voltage aggressively scales with each technology generation, making the delivery of a high quality supply voltage to noise sensitive circuit blocks highly challenging. Moreover, supply voltage is sometimes tuned in time to achieve lower power consumption, which is called dynamic voltage scaling. The development of Nano watt LSIs is expected to lead to the expansion of next-generation power-aware applications such as life-assist medical devices, environmental sensors, and wireless sensor networks [1], [2]. Because they must operate for a long time within less-than-ideal energy supply from micro batteries, so there is a need in designing LSIs that operate with extremely low power dissipation. To develop such LSIs, we must first develop voltage reference circuits because they are one of the most fundamental analog building circuits. Here, process, voltage, and temperature (PVT) variation-tolerant voltage reference circuits is described that can operate at several tens of Nano watts or less. Bandgap reference (BGR) circuits are widely used in modern LSIs to generate a reference voltage on chips. The generated voltage is used for various analog signal processes.

Though several BGRs have been developed, the power dissipations of most of them does not exceed nanowatt power [3]–[7] and have not been significantly reduced. One reason for this is the use of resistors. The resistors

in most reference circuits are used to generate current or voltage to control the temperature characteristics of the output reference voltage [3]–[9]. When we use a moderate value for resistance, sufficient current for the resistors is required and power dissipation therefore cannot be reduced. Even if we use a large value for resistance, the resistors will occupy a large area of the silicon. Resistor-less voltage reference circuits that operate at Nano watt power have been reported [10]–[12]. However, the output reference voltages of these circuits are based on the threshold voltage of MOSFETs, the voltages will change with process variations. Therefore, they are not suitable for use as voltage reference circuits. This paper presents a nanowatt BGR circuit that does not use resistors. The proposed BGR consists of a nano-ampere current reference circuit, a bipolar transistor, and proportional-to-absolute-temperature (PTAT) voltage generators. Because the circuit only consists of MOSFETs except for the bipolar transistor, it can generate a bandgap voltage without resistors. In addition, a sub-BGR circuit that generates voltage lower than 1.2 V is also presented. The proposed sub-BGR uses a voltage divider. The voltage divider accepts the base-emitter voltage of the bipolar transistor and generates a sub-1-V reference voltage in combination with the PTAT voltage generators. Therefore, the proposed sub-BGR is useful as a reference circuit in sub-1-V LSIs.

2. Architecture

2.1 BGR CIRCUIT

Fig. 1 shows the architecture of the proposed BGR circuit. It consists of a nano-ampere current reference circuit, a bipolar transistor, and a PTAT voltage generator. PTAT voltage in conventional BGR circuits is generated by using bipolar transistors and resistors. Fig. 2 shows the PTAT voltage generator consisting of a differential pair with a current mirror. When the MOSFETs operate in the sub-threshold region, gate-to-gate voltage in this circuit can be expressed as

$$\begin{aligned} VGG &= VOUT - VIN \\ &= VGS,D2 - VGS,D1 \\ &= VTH + \eta VTH \ln\left(\frac{ID2}{KD2I0}\right) - \left(VTH + \eta VT \ln\left(\frac{ID1}{KD1I0}\right)\right) \\ &= \eta VT \ln\left(\frac{KD1KM2}{KD2KM1}\right) \end{aligned} \quad (1)$$

Where KD1 and KD2 correspond to aspect ratios in the differential pair, KM1 and KM2 correspond to aspect ratios in the PMOS current mirror. Therefore, PTAT voltage can be generated by making KD1KM2/KD2KM1 > 1

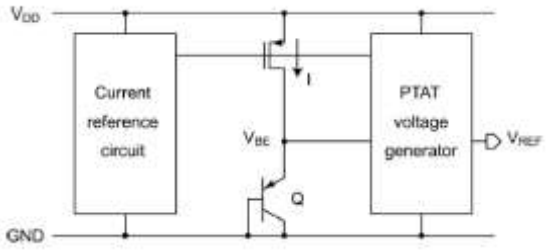


Fig.1 Architecture of BGR circuit

The nano-ampere current reference circuit generates a 10-nA current and supplies it to the others. Fig. 3 is a schematic of a nano-ampere a current reference circuit [15]. The circuit consists of a bias voltage circuit, the PTAT voltage generator, and a current source circuit. All MOSFETs operate in the subthreshold region except

for the MOS resistor MR that operates in the strong-inversion and deep triode regions. The gate length L and the gate width W of MR and MB are the same, and they are biased at the same current. The PTAT voltage generator adds a voltage to the gate–source voltage of MB in order to increase that of MR. The value of the MOS resistor is defined by

$$I = \mu COXK(VGS - VTH)VDS \tag{2}$$

The bipolar transistor accepts the current through a current mirror and generates a base-emitter voltage,

$$VBE = VT \ln\left(IS + \frac{1}{IS}\right) \approx VT \ln\left(\frac{I}{IS}\right) \tag{3}$$

Where IS, is the saturation current of the bipolar transistor [14].Because VBE decreases linearly with temperature and simplified as

$$VBE = VBGR - \gamma T \tag{4}$$

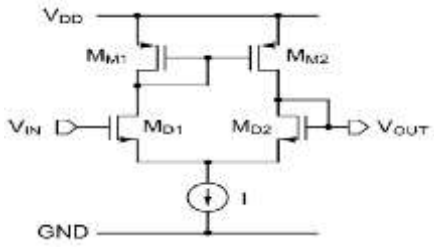


Fig.2 PTAT voltage genertor consisting of differential pair circuit

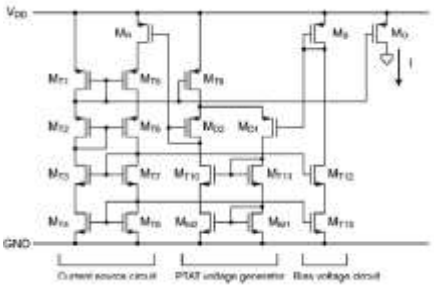


Fig.3schematic of nano-ampere current reference circuit

The temperature coefficient of VBE has a negative dependence on temperature, the PTAT voltage generator is used to cancel out this dependence. However, the nonlinearities can be compensated for if we use a technique of curvature compensation. The bias current of the bipolar transistor also determines the accuracy of VBE. The PTAT voltage generator in Fig. 2 supplies voltage which has a positive dependence on temperature.

$$VREF1 = VBE + \sum_{i=1}^{N} VGG, i \tag{5}$$

$$VREF1 = VBGR \tag{6}$$

Therefore, the condition can be obtained by appropriate choice of the aspect ratios of the transistors in the differential pairs and current mirrors, and of N.

2.2 Sub-BGR CIRCUIT

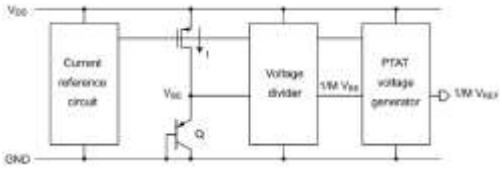


Fig.4 Architecture of proposed SUB-BGR circuit

The bandgap voltage of silicon is larger than 1.2 V; BGR circuits require more than 1.2 V of supply voltage. Here, a voltage reference circuit that operates at sub-1-V power supply is presented. Fig. 4 shows a block diagram of the proposed sub-BGR circuit. The circuit uses a voltage divider circuit. The voltage divider circuit divides the base-emitter voltage. The output voltage of the voltage divider can be expressed as

$$\frac{VBE}{M} = \frac{VBGR}{M} - \frac{\gamma}{M}T \tag{7}$$

where M is the division ratio of the divider. Then, the PTAT voltage generator is also used to cancel the negative dependence on temperature of VBE/M.A zero temperature coefficient voltage is obtained in a same way to that of the BGR circuit by designing the aspect ratios ,

$$VREF2 = \frac{VBGR}{M} \tag{8}$$

If VBGR is divided by M after it is generated, supply voltage of the circuit requires more than 1.2 V. This is because the circuit has to generate VBGR in advance. However, because the proposed sub-BGR circuit divides the base-emitter voltage and output reference voltage VREF/M is lower than 1.2 V, the sub-BGR circuit can operate at sub-1-V power supply.

3. EXPERIMENTAL RESULTS

Figs. 5 and 6 show the schematics for the proposed BGR and Sub-BGR circuits. A cascade configuration was used in the circuits to reduce dependence on supply voltage. Five differential pairs were used in the BGR design and three pairs in the sub-BGR circuit. A zero temperature coefficient voltage can be obtained by designing the aspect ratios in the differential pairs and the current mirror

$$VREF1 = VBGR \tag{9}$$

We used a source-follower circuit as a voltage divider circuit in the sub-BGR. The voltage divider circuit divided the base-emitter voltage in half. Each body terminal of the nMOSFETs in the source-follower circuit was connected with their source terminal to avoid the body effect of the transistor. Here the gate and substrate leakage currents are ignored because the leakage currents are smaller than the sub-threshold current in the process. Then, three differential pairs were used in the sub-BGR to cancel the negative dependence on temperature of VBE/2. We used two pMOS differential pairs as first PTAT voltage generators VBE/2 because would have been too low to apply an nMOS PTAT generator. Therefore, a zero temperature coefficient voltage can be obtained and the voltage can be written as,

$$VREF2 = \frac{VBGR}{M} \tag{10}$$

The circuits for driving capabilities should not be directly connected to resistive loads because of their poor driving current. Bias current in the last stage of the PTAT generators should be increased if we have to drive

resistive loads and/or large capacitive loads. However, the increase in bias current leads to high power dissipation.

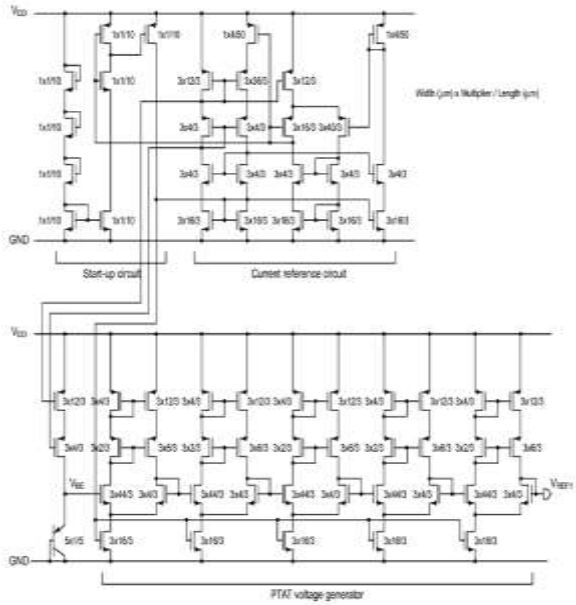


Fig.5 schematic of proposed BGR circuit

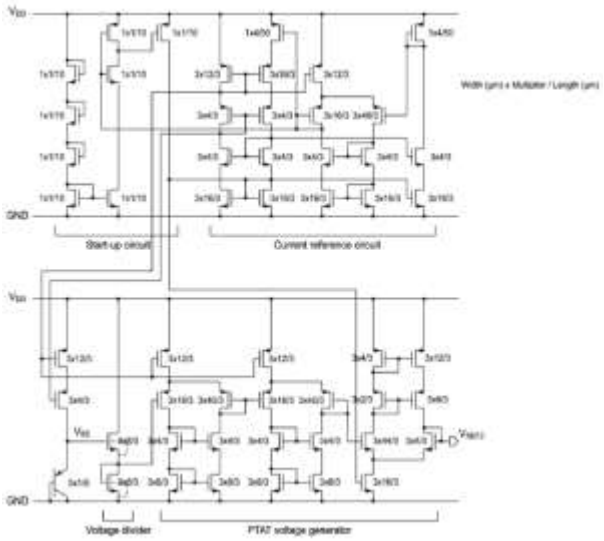


Fig .6 schematic of proposed Sub-BGR circuit

4. SIMULATION AND RESULTS

When the bipolar transistor accepts the constant currents, VBE at absolute zero temperature were almost equal to the material bandgap voltage (1.2V). As the operating current increased with temperature, VBE increased gradually. As a result, VBE at absolute zero temperature became lower than the material bandgap voltage. The circuit is implemented by using tanner EDA tool and checked its simulation results. From the simulation results it is clear that, sub-BGR circuits are more efficient than BGR circuits in power as well as in area.

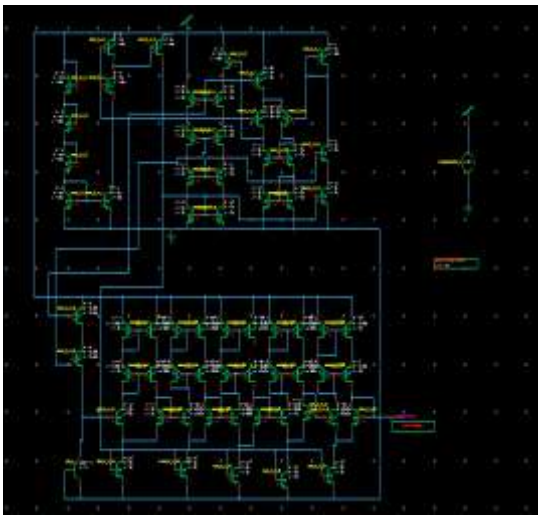


Fig.7 schematic of proposed BGR circuit simulated in tanner EDA tool

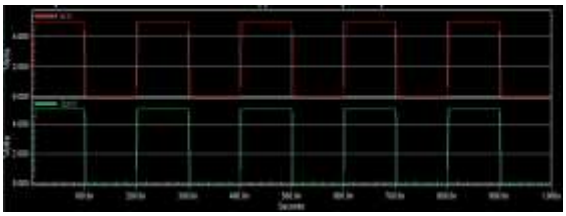


Fig.8 simulated output of proposed BGR

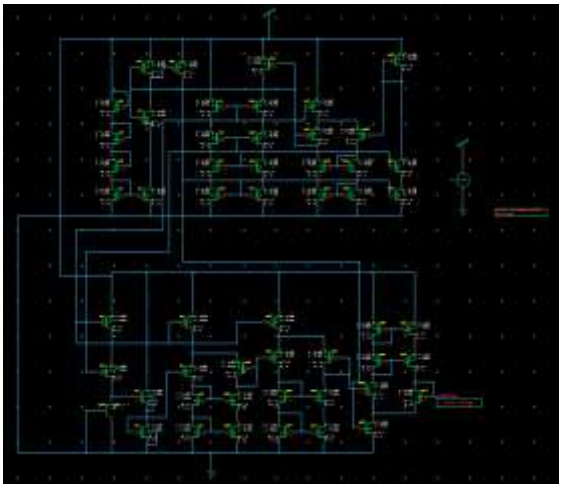


Fig.9 schematic of proposed Sub-BGR circuit simulated in tanner EDA tool

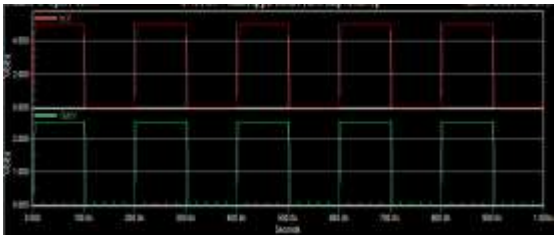
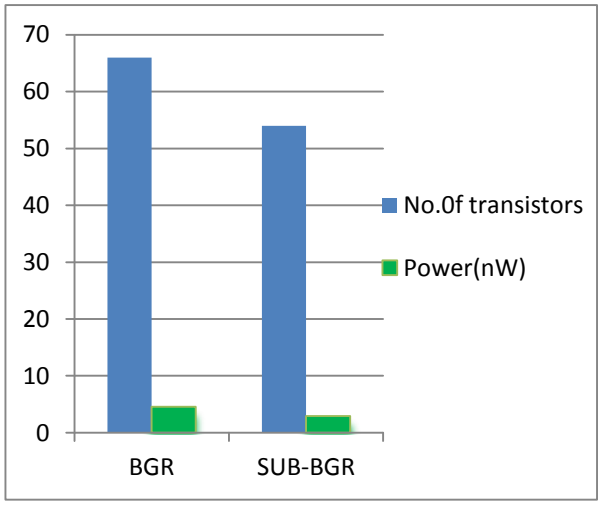


Fig.10 simulated output of proposed Sub- BGR

ANALYSIS REPORT

Circuits	No.of transistors	Power(nW)
BGR	66	4.608
SUB-BGR	54	2.952



V. CONCLUSION

BGR and sub-BGR circuits for extremely low-power LSIs were presented. The circuits consisting of MOSFETs and bipolar transistor thus generated reference voltages without resistors. Because the sub-BGR circuit divides the output voltage of the bipolar transistor, it can operate at sub-1-V power supply. The experimental results demonstrated that the sub-BGR circuit is more efficient than BGR circuit both power as well as in area.

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