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DESIGN OF 16-BIT CARRY-LOOKAHEAD ADDER AND 8-BIT KOGGE-STONE ADDER USING GDI LOGIC

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Abstract

Addition is a fundamental arithmetic operation and is the base of many other commonly used arithmetic operations such as subtraction, multiplication, division and, multiply and accumulate (MAC) in most of these systems. The 1-bit Full Adder cell is the building block of an arithmetic unit of a system. There are several full adder designs designed so far to improve the performance. However, each design suffers from specific disadvantage. The adder design which has good driving capability acquires more power and the design which consumes less power will have more delay. This paper proposes Gate Diffusion Input (GDI) Logic based 16-bit carry-lookahead adder and 8-bit Kogge-stone adder which consumes low power, operates at high speed and has less area.

Keywords: GDI Structure, Low power, Carry-lookahead adder, Kogge-stone adder.

1. Introduction

The demand and popularity of portable electronics is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. Power consumption and area reduction of logic and memory have become primary focuses of attention in VLSI digital design. Power is the limiting factor in both high performance systems and portable applications. Die area directly affects the device size and cost. Since the introduction of the standard CMOS Logic in early 80s, many design solutions have been proposed to improve power dissipation, area and performance of digital VLSI chips. Gate Diffusion Input (GDI) design methodology was introduced as a promising alternative to Static CMOS Logic. Originally proposed for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes, GDI methodology allowed implementation of a wide range of complex logic functions using only two transistors. It was shown, that area and dynamic power of GDI combinatorial and sequential logic were significantly reduced, as compared to standard CMOS implementations.

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2. Review of Existing Techniques

2.1 Carry-Lookahead Adder (CLA)

CLA is used in most ALU designs. It is faster especially in adding large number of bits. . A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bit. Carry-Lookahead Adder is able to generate carries before the sum is produced using propagate and generate logics to make addition much faster.

Generate, $G_i = A_i$ AND B_i (1)

Propagate, $Pi = (A_i$ XOR $B_i)$ (2)

The general architecture of 16-bit CLA is shown in Figure 1. Carry-Lookahead adder and Kogge-stone adder were previously designed using static CMOS logic designs. The static digital designs are mostly based on CMOS NAND and NOR gates. The previously proposed designs suffer from high power consumption and more area [Jagannath samanta *et al*., 2013].

The proposed GDI based carry-lookahead adder is compared with a carry-lookahead adder designed using ULPD (Ultra Low Power Diode) and full swing transistor based carry-lookahead adder design. The CLA adder designs have various modules. The base module will provide propagate and generate as outputs by accepting two inputs. These base propagate and generate outputs will act as inputs to another block (PG) in the hierarchy. Local Carry Generate module is built after this block using base propagate and generate outputs and by using input carry. A 2-bit CLA can be made by using PG and LCG (Local Carry Generate) modules. ULPD based CLA uses Ultra Low Power Diode which is used to provide full swing and to obtain low power. This diode consists of an NMS and PMOS whose gates are connected in series [David Levacq *et al*., 2007]. This diode reduces leakage current. ULPD is shown in Figure 2 [Hassoune. I *et.,al* 2010]. Full Swing transistor based CLA uses F1 and F2 gates which are shown in Figure 3. These gates use swing restoring transistors to improve the output swing. These transistors will have a diffusion input as nMOS for F1 and pMOS for F2. These two adder designs consume more power.

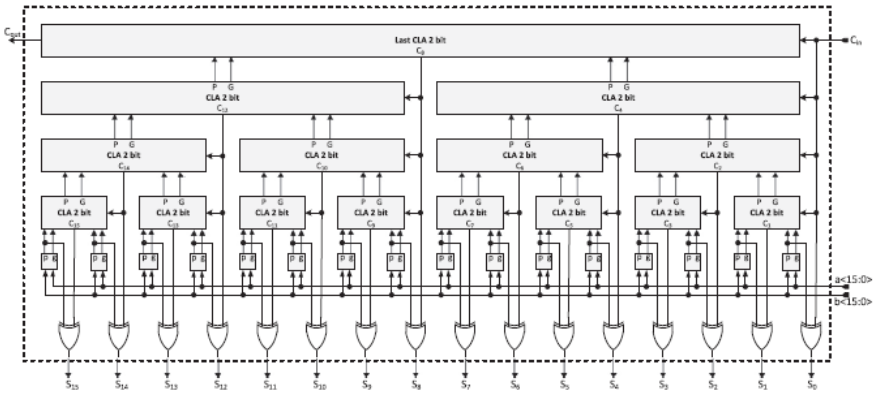

Figure 1: General architecture of CLA

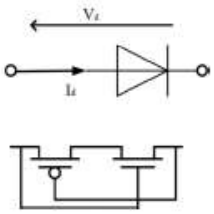

Figure 2: ULPD

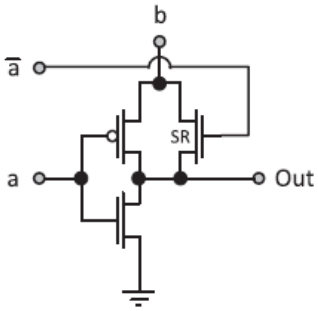

Figure 3(a): F1 gate

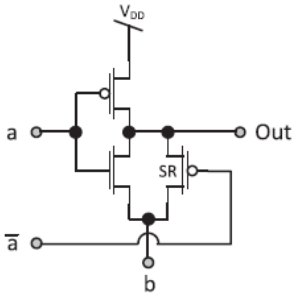

Figure 3(b): F2 gate

2.2 Kogge-Stone Adder

It is the fastest adder used in industries. It is the parallel prefix form of carry-lookahead adder. It consists of black cell and grey cell [Adilakshmi siliveru *et al*., 2013]. The general architecture of 8-bit Kogge-Stone adder is shown in Figure 4.
There are three stages of operation.

2.2.1 Preprocessing stage

In this stage, propagate and generate terms are obtained.

Propagate, P = A XOR B (3)
Generate, G = A AND B (4)

2.2.2 Carry-Lookahead network

In this network, (Pij, Gij) is generated from (Gi, Pi) and (Gj, Pj)

$P_{i:j} = P_{i:k+1}$ AND $P_{k:j}$ (5)
$G_{i:j} = G_{i:k+1}$ OR ($P_{i:k+1}$ AND $G_{k:j}$) (6)

2.2.3 *Post Processing*

Sum and carry are obtained.

Sum = Pi XOR Carry in (7)
Carry= $G_{i:0}$ OR (Cin AND $P_{i:0}$) (8)

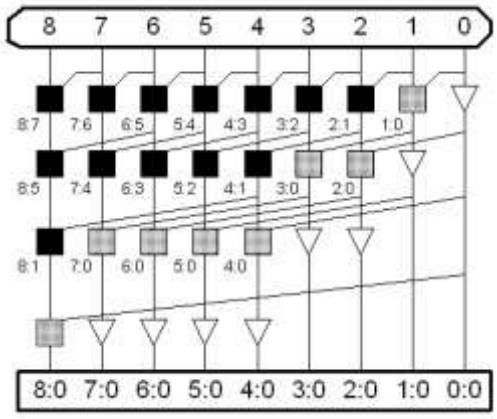

Figure 4: General architecture of 8-bit Kogge-Stone adder

3. Overview of GDI cell

The basic GDI cell [Arkadiy Morgenshtein *et al.*, 2002] is shown in Figure 5 while the Truth-Table of basic GDI cell is shown in Table 1. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences. The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/ drain of NMOS).Bulks of both NMOS and PMOS are linked to N or P, so it can arbitrarily be biased at contrast to a CMOS inverter. These features give the GDI cell two extra input pins to use, which make the GDI design more flexible than usual CMOS design.

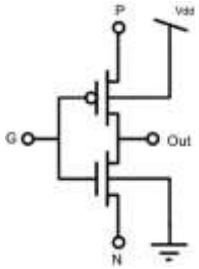

Figure 5: Basic GDI Cell

Table 1: Truth table of GDI cell

N	P	G	Out	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}+B$	F2
B	B	A	$A+B$	OR
1	0	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
0	1	A	$\overline{A}$	NOT

Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method. GDI is suitable for designing fast, Low-Power circuits, using a reduced number of transistors (as compared to CMOS and Pass Transistor

Logic techniques), while improving logic level swing and static power characteristics [Jiang.Y *et al*., 2004, Lee P.M *et al*., 2007 and Narendra Lakhani *et al*., 2013].

4. Proposed Adder Circuits

4.1 Carry-Lookahead Adder (CLA)

The base pg unit is implemented using (9) and (10)

p = a xor b, GDI XOR gate (9)

g = a and b = $\overline{F2(a,\bar{b})}$ (10)

The PG unit is implemented using (11) and (12)

P = $p_1 p_0$ = $F1(\overline{P1},P0)$ (11)

G = $g_1 + g_0 p_1$ = $\overline{F1(g1,F2(g0,\overline{p1}))}$ (12)

The local carry generate block (LCG) is implemented according to (13)

Cloc = $g_0 + p_0 c_{in}$ = $\overline{F1(g0,F2(Cin,\overline{P0}))}$ (13)

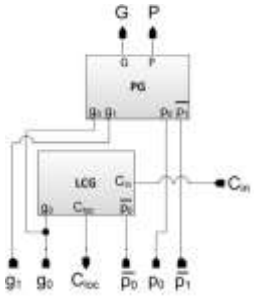

Figure 6: 2-bit CLA

Figure 6 shows 2-bit CLA block consisting of PG and LCG unit. The global carry generate block is shown in Figure 7 and the output is implemented according to (14)

Cout = G1 + P1G0 + P1P0Cin = $F2(\overline{P1G0 + G1}\ , P1P0Cin)$

= $F2\left(\overline{F2(\overline{P1G0},G1)},F1(\overline{P1P0},Cin)\right)$

=$F2\left(\overline{F2\left(\overline{F1(\overline{P1},G0)},G1\right)},\ \overline{F1F1(\overline{P1},\overline{P0}),Cin)}\right)$ (14)

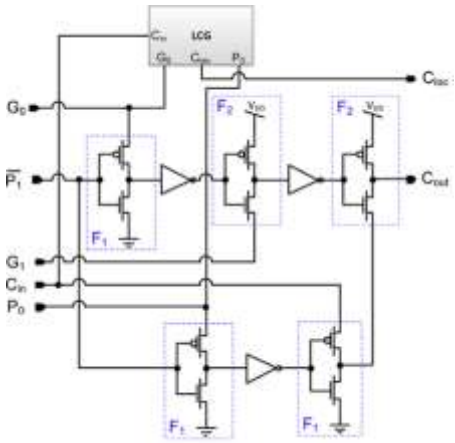

Figure 7: Last CLA [Arkadiy Morgenshtein et al., 2013]

4.2 Kogge-Stone Adder

Kogge-stone adder generates carry signals in O (log n) time. It is the fastest adder design and is the common design for high performance adders in industry. It can also be used to implement other functions [Madhu Thakur *et al*., 2013]. Kogge-stone adder consists of black cell and grey cell. The black cell shown in Figure 8

consists of two AND gates and an OR gate which will produce propagate and generate terms. The Grey cell shown in Figure 9 consists of an AND gate and an OR gate to provide generate term.

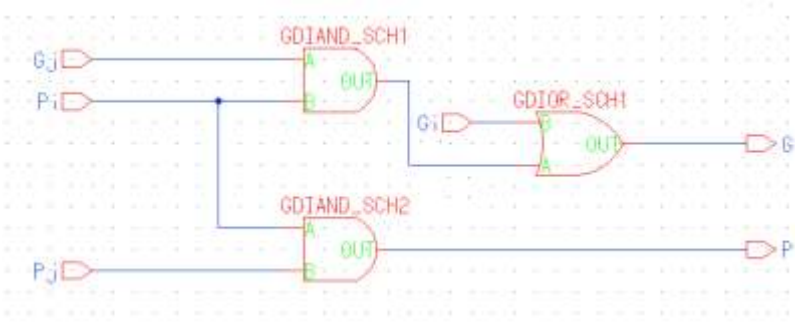

Figure 8: Black cell

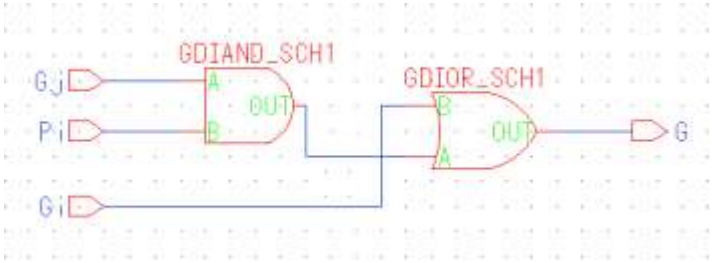

Figure 9: Grey cell

5. Simulation Results and Analysis

5.1 simulation Results

The simulation result is similar to that of one bit full adder. When A, C are high and B is low, SUM is low and COUT is high. When any one of the three inputs is high, SUM will be high.

5.2 Analysis

Table 2 shows the analysis report of various CLA adder designs. Table 3 shows the analysis report of various Kogge-Stone adder designs. From the tables, it is obvious that GDI based CLA and GDI based Kogge-Stone adders have low power, less delay, utilizes minimum number of transistors and thereby has reduced area.

Table 2: Analysis Report of various CLA adders

Various CLA adder designs	Power (pW)	Delay (pS)	PDP(J)	No. of components
Full swing transistor based CLA	2133.72	203.10	433358.73	958
ULPD based CLA	80.07	205.43	16450.81	890
GDI based CLA	**69.77**	**127.15**	**8871.56**	**658**

The graphical representations for power, delay and PDP for various CLA adder designs are shown in Figure 10, Figure 11 and Figure 12 respectively.

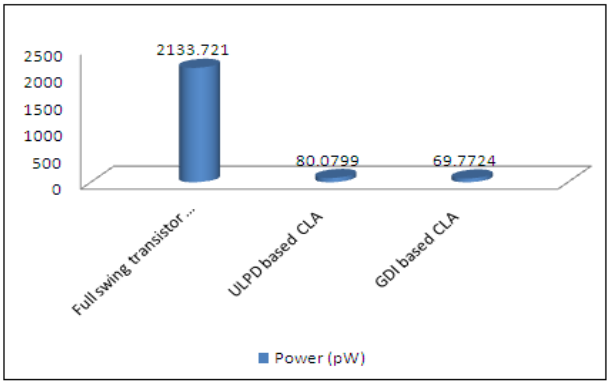

Figure 10: Comparison result of power dissipation (various CLA adder designs)

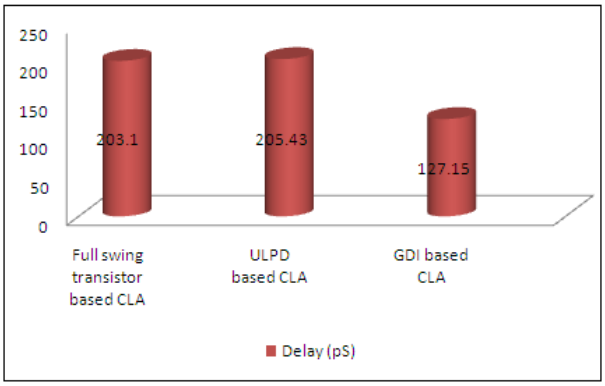

Figure 11: Comparison result of delay (various CLA adder designs)

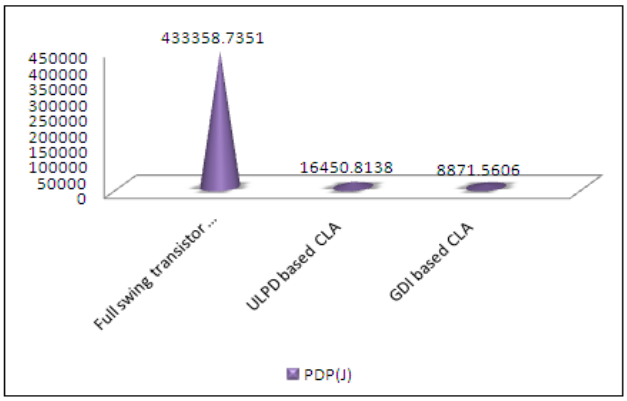

Figure 12: Comparison result of PDP (various CLA adder designs)

Table 3: Analysis Report of various Kogge-Stone adders

Various Kogge stone adder designs	**Power (pW)**	**Delay (pS)**	**PDP (J)**	**No. of components**
Primitive gate based Kogge stone adder	42.21	547.11	23095.31	588
Transistor based Kogge stone adder	37.98	563.38	21400.77	442
GDI based Kogge stone adder	**20.85**	**471.57**	**9835.29**	**390**

The graphical representations for power, delay and PDP for various Kogge-Stone adder designs are shown in Figure 13, Figure 14 and Figure 15 respectively.

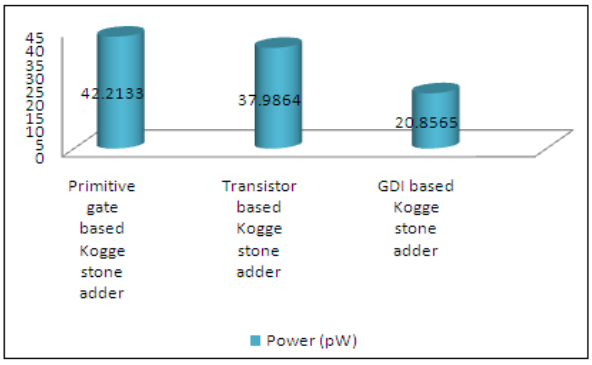

Figure 13: Comparison result of power dissipation (various Kogge stone adder designs)

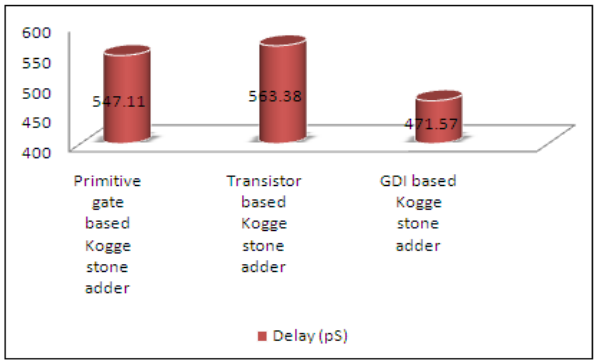

Figure 14: Comparison result for delay (various Kogge-Stone adder designs)

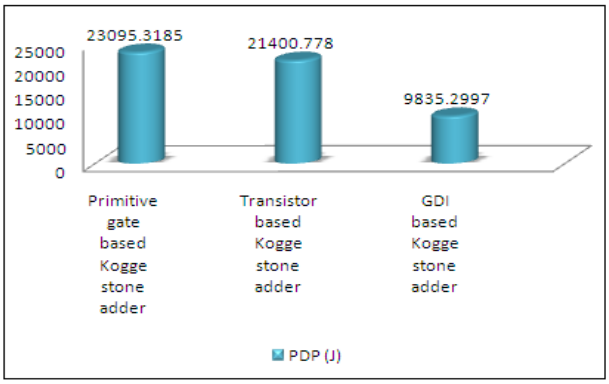

Figure 15: Comparison result of PDP ((various Kogge stone adder designs)

6. Conclusion

The proposed GDI based CLA adder and GDI based kogge stone adder utilize GDI structure as its main cell which is proved to be one of the lowest power consumer cells that not only is suitable for designing fast, Low-Power circuits but also improves logic level swing.. After analyzing the performance of GDI based CLA adder and GDI based Kogge stone adder using Mentor Graphics EDA tool under 180 nm technology, GDI based CLA is found to occupy low power, less delay and less number of transistors compared to ULPD based CLA and full swing transistor based CLA, GDI based Kogge stone is found to occupy low power, less area and less number of transistors compared to primitive gates based and transistor based Kogge-Stone adders. The proposed adder designs can be applied to any operation used in VLSI applications such as DSP (Digital Signal Processing), micro processors, video and image processors. The work can be further extended to any benchmark circuits, where they can be converted into standard cells and realized in an Integrated Circuit.

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