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POWER EFFICIENT MEMORY DESIGN USING DOMINO LOGIC

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Abstract

In this paper a power efficient memory file register is designed using Current comparison based domino (CCD) logic. This domino logic is used in designing the Local & Global bit line (LBL & GBL) of the memory file. An 8*8 register memory file is designed and the LBL & GBL are designed by using both CCD domino logic and the basic Standard Footless Domino Logic (SFLD) and the power dissipation and such results are compared. Also the CCD logic is enhanced further by including Clock Gating technology & the memory file is designed using this logic

Keywords: Current comparison, Domino logic, Register memory file, Clock gating, Local bit line, Global bit line.

1. Introduction

Domino logic circuits are most widely used in many applications. One among such applications is the register file design. The register files are commonly used in microprocessors. These register files need the domino logics for designing the Local and global bit lines (LBL & GBL). The domino logic thus used has large number of leaky paths which contributes towards high power dissipation. To avoid that a new domino logic technique called Current comparison logic is used.

2. Body of the article

There are many existing domino techniques. The first technique proposed was the standard footless domino logic SFLD) [1]. This is the most popular dynamic logic. Here a pMOS transistor is used which works as a keeper transistor. The main reason for the keeper transistor is to avoid unnecessary discharge of the dynamic node which occurs mainly due to leakage current and charge sharing of the Pull Down Network (PDN). But because of increasing the size of the keeper transistor contention of current between the keeper transistor and the evaluation network occurs which in-turn increases the power consumption and delay of the circuit. H. Suzuki, C. Kim and K. Roy proposed a logic called Diode Partitioned Domino logic (DPD) in June 2005 [3] for fast tag comparators. This method reduces the parasitic capacitance. This helps in having small keeper in wide fan-in gates. The diode circuit is improved by a diode which boosts the gate voltage of nMOS diode. But this type suffers from power dissipation. M.H Anis, M.W Allam and M.I. Elmsary in April 2002 [2] proposed a logic called High Speed Domino logic (HSD). This logic reduces the current drawn through pMOS keeper transistor and the nMOS PDN. This helps avoiding performance degradation and leakage current. But area overhead and power overhead occurs. H. Mahmoodi and K. Roy proposed Diode Footed Domino logic (DFD) in March 2004 [4]. A transistor in diode combination is added in series. This transistor is added as a footer transistor to the evaluation network. This leads to increased robustness. A. Alvandpur, R. Krishnamoorthy and K. Sourty proposed a logic called conditional keeper domino logic (CKD) in Jan 2007 [5]. This model consists of small and large keeper transistors. The disadvantages are increased delay and power dissipation due to upsizing. Ali Peravi and Mohammed Asyaei proposed a robust low leakage controlled keeper based domino in 2012 [6] which works on reducing the leakage current. But this method suffered seriously from

efficiency issues in terms of area and delay. The Fig 1 shows the SFLD logic.

3. CURRENT COMPARISON BASED DESIGN

The current comparison based domino logic uses the following concepts to reduce the power dissipation.

1) Stacking effect
2) Very few pull up transistors to reduce switching
3) Current comparison logic for correct switching of keeper transistors in order to avoid current contention between keeper transistors

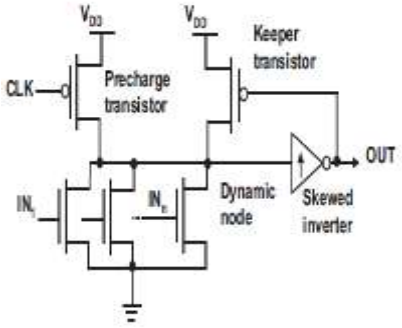

Figure 1. STANDARD FOOTLESS DOMINO LOGIC

The Fig 2 shows the Current comparison based domino logic

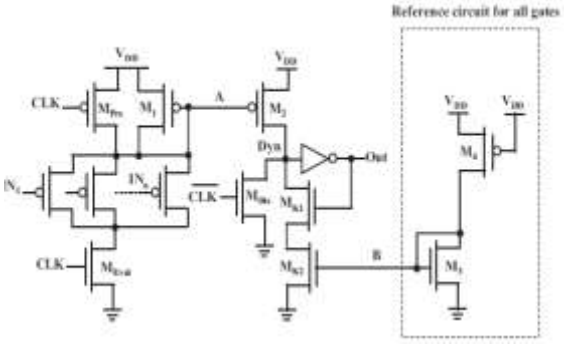

Figure 2. CURRENT COMPARISON BASED DOMINO LOGIC

3.1 REGISTER FILE DESIGN

The high performance microprocessors require multi-ported register files to execute independent instructions in parallel by multiple functional units. Local (LBL) and Global (GBL) bit lines of register files are typically implemented by wide dynamic circuits. Multi ported register files are highly advantageous than single port register files because of multiple reading / writing capability from / to the ports. The FIG 3 shows the complete 8*8 register file architecture [7].

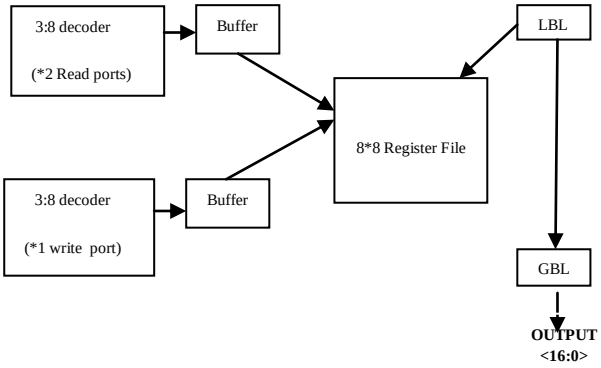

Figure 3. 8*8 REGISTER FILE

As shown in Fig. 3, the organization of the 2-read,1-write ported 8-word register file is used to compare several circuit techniques. The 3:8 decoder is used for both the ports.

The full-swing local bit line (LBL) implemented by the standard footless domino (SFLD) & CCD are shown in Fig. 4(a) and (b). FIG 5 represents the Local bit line using SFLD Each read port needs a LBL which forms a dynamic 8-way AND–OR. During read cycle, data from the storage cell is read by two transistors per word (M1 and M2) on each LBL. The GBL circuits are 8-input OR gates. These circuits deliver the 8 bit word per read port from bit cells.

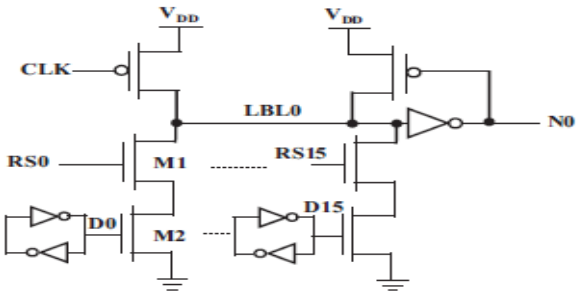

Figure 4 (a). Local Bit Line using SFLD

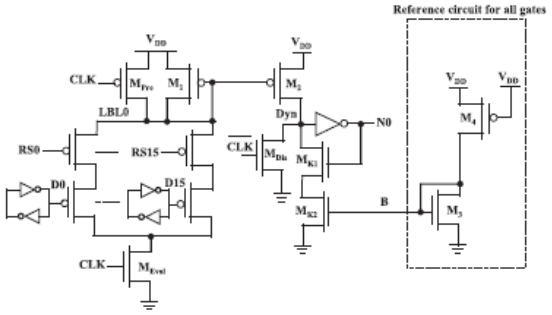

Figure 4(b). Local Bit Line using CCD

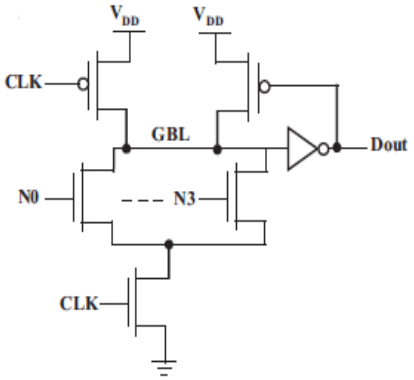

Figure 5. Global Bit Line

3.2 REGISTER FILE BIT CELL DESIGN

The Fig. 6 shows the register file bit cell, in which one read ports on each side of the storage cell is inserted to provide symmetric loading during cell write for optimal stability. Demand for complement of the input data is removed by using an extra NMOS pass transistor.

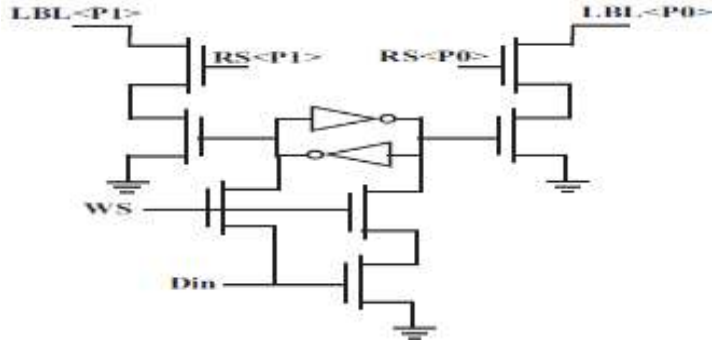

Figure 6. SYMETRIC REGISTER FILE BIT CELL

4. CLOCK GATED CCD DOMINO LOGIC

Along with normal CCD logic, the clock gating concept is included. The advantage of clock gating technique is that by including an AND gate with one input as the clock signal and other one as control input, at times where clock signal is not needed, by disabling "En" enable signal to the AND gate, the clock signal to the logic can be disabled (in case of Global clock). This saves power dissipation due to "always ON" clock signal. The structure is depicted in FIG 7.

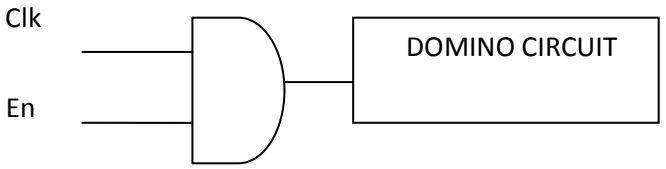

Figure 7. CLOCK GATED DOMINO LOGIC

5. RESULTS AND COMPARISION

The simulation is done using MENTOR GRAPHICS EDA tool at 180 nm technology and ami05.mod model file. The Table.1 exhibits power dissipation comparison between SFLD based LBL and GBL & CCD based LBL and GBL. The table 2 exhibits power dissipation comparison between normal CCD logic and Clock gated CCD logic the Table 3 compares the power dissipation between 8*8 Register file designed using SFLD, CCD & clock gated CCD domino logic. From all the tables it can be inferred that the Clock Gated domino logic proves to be more efficient than the SFLD and CCD logics with reduced power dissipation. The Figure 8 shows the 8*8 register file memory design done using MENTOR GRAPHICS EDA tool.

TABLE 1.POWER DISSIPATION COMPARISON BETWEEN SFLD and CCD BASED LBL and GBL schemes

LOGIC	POWER DISSIPATION OF LBL	POWER DISSIPATION OF GBL
SFLD	2.107 µW	2.86 µW
CCD	123.14 nW	11.57 nW

TABLE 2.POWER DISSIPATION COMPARISON BETWEEN CCD and CLOCK GATED CCD LOGIC

NO.OF.INPUTS	POWER DISSIPATION OF CCD LOGIC	POWER DISSIPATION OF CLOCK GATED CCD LOGIC
4 INPUT	1.6887 µW	41.1156 nW
8 INPUT	842.820 µW	66.4306 µW
16 INPUT	880.177 µW	645.0550 µW

TABLE 3 POWER DISSIPATION COMPARISON BETWEEN SFLD, CCD AND CLOCK GATED CCD BASED 8*8 REGISTER FILE MEMORY DESIGN

LOGIC	POWER DISSIPATION OF 8*8 REGISTER FILE MEMORY DESIGN
SFLD	108.656 MW
CCD	46.172 nW
CLOCK GATED CCD	294.66 µW

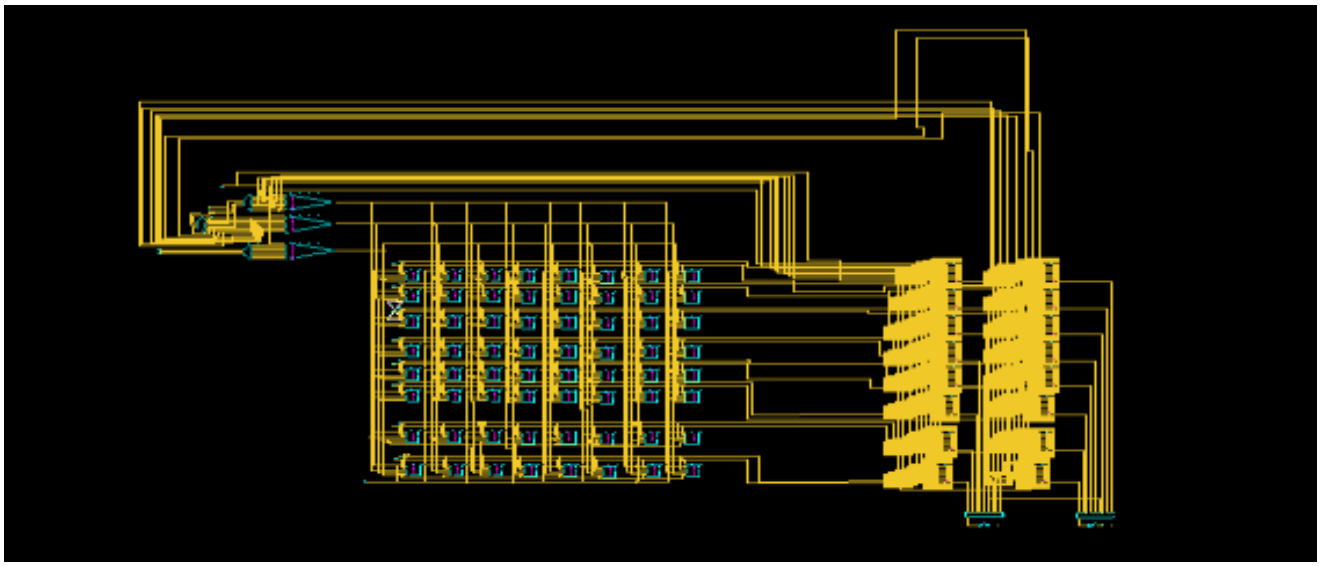

Figure 8. 8*8 REGISTER FILE MEMORY DESIGN

6. CONCLUSION

Multi-ported register files and larger caches for higher performance processors are more power- hungry devices in modern super scalar microprocessors. The demand for low power dissipation designs has strongly increased along with the recently growing mobile-market. This paper introduces an efficient approach to reduce the power consumption in register files using Clock gated current comparison based domino logic. A 8*8 memory register file is designed and simulation results prove that while comparing with the SFLD and CCD LOGIC the clock gated CCD logic is very efficient in terms of low power dissipation.

REFERENCES

[1] J.M.Rabey, A.Chandrasekaran and B.Nicolic, Digital Integrated Circuits: A Design Perspective, 2nd Upper Saddle River, NJ: Prentice-Hall, 2000.

[2] M.H. Anis, M.W.Allam and M.I.Elmasry, "Energy Efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies", IEEE Trans. Very Large Scale (VLSI) Syst.,vol.10, no.2,71-78,Apr.2002

[3] C.H.Kim, K.Roy, S.Hsu, R.Krishnamoorthy and S.Borkar, "A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits ", IEEE Trans. Very Large Scale (VLSI) Syst.,vol.14,no.6,pp.646-649,Jun.2005.

[4] H.Mahamoodi and K.Roy, Diode Footed Domino: A leakage tolerant high fan-in dynamic circuits design style", IEEE Trans.Circuits Syst.1, Reg. Papers, vol.51,no.3,pp.495-503,Mar 2002.

[5] A.Alvandpur, R.Krishnamoorthy, K.Sourty and S.Y.Borkar, "A sub-130 nm conditional keeper technique" IEEE J.Solid-State Circuits Vol.37, n0.5, pp, 633-638, Jan 2007.

[6] A.Peravi and M.Asyaei, "Robust low leakage controlled keeper by current comparison domino wode fan-in gates, integration", VLSI J., Vol.45, no.1, pp.22-32,2012

[7] A. Alvandpur, G. Balamurugan, R.K. Krishnamoorthy "A 130 nm 256*32 bit leakage tolerant register file", IEEE Journal of Solid State Circuits, Vol.37, NO.5, May 2002.