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DESIGN AND ANALYSIS OF LOW POWER LEVEL SHIFTER

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Abstract

Level shifters play critical roles in ultra low-voltage circuits and systems. a new low power level shifter (LS) is presented for robust logic voltage shifting from near/sub threshold to above threshold domain. The new circuit combines the multi threshold CMOS technique along with novel topological modifications to guarantee a wide voltage conversion range with limited static power and total energy consumption. Therefore, this paper presents a novel level shifter, of which the operating range is from a deep sub threshold voltage to the standard supply voltage and includes upward and downward level conversion. The proposed level shifter is a hybrid structure comprising a modified Wilson current mirror and generic CMOS logic gates. power is main constraint in a level shifter. Modified level shifter using cascaded current mirror circuit. In addition to the operating range delay, power consumption, and duty cycle of the proposed level shifter

Keywords: level shifter, Wilson current mirror

I. Introduction

The most effective and direct way to reduce power dissipation in digital LSIs is to reduce their supply voltage because of their quadratic dependence of the power dissipation on the supply voltage. Several low-power design techniques have been investigated. First, previous sub-threshold LSs may exhibit timing issues when the input and output levels are close. Ultra-low-voltage (ULV) processors and memories usually support sub-threshold and supra-threshold operations for enabling energy and performance trade-offs. Both wide-range and close-range level conversion are required to achieve this flexibility. When input and output levels are close, previous sub-threshold LSs may have considerable skews in rising and falling delays because the drive strength of the PUNs was reduced. Although weak pull-up strength is favorable when input level is low, the rising delay increases considerably when the input level becomes high. Therefore, the operating range is confined. With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become major design consideration for VLSI circuits and system. With increase in power consumption, reliability problem also rises and cost of packaging goes high [3]. Power consumption in VLSI circuit

consists of dynamic and static power consumption. Dynamic power has two components i.e. switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [4].The static power of CMOS circuits is determined by the leakage current through each VLSI circuits can be reduced by scaling supply voltage and capacitance [4]. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage currents originate
[5]. component of power consumption must be given due consideration if current trends of scaling of size and supply voltage need to be sustained. This paper presents novel LS that use a modified Wilson current mirror hybrid buffer (MWCMHB). The proposed MWCMHB LS was designed for full-range and bidirectional level conversion. The term "full range" indicates that the minimal operating voltage can be deep sub-threshold, close to the minimal supply voltage of digital circuits, and the maximal operating voltage is the standard supply voltage defined in a transistor technology. In addition to the operating range, the delay, power consumption, and duty cycle of LSs were carefully considered. The energy efficiency of wide-range level conversion was examined. The low slew rate of sub-threshold signals may lead to a long transition period and consume high short-circuit power [14]. To reduce this power consumption, robust sub-threshold LSs require amendments with proper voltage assignment.

II. Existing System

The existing CMOS level shifters are broadly classified into two main categories: 1) Dual Supply Level Shifters (DSLS) and 2) Single Supply Level Shifters (SSLS). The advantages of SSLS over DSLS have been illustrated on the grounds of pin count, congestion in supply routing, complexity and overall system cost.

SSLS circuits do not require access to the lower supply voltage other than the signal to be converted. However in our target applications, all level shifters have unhindered access to both supply voltages without increasing routing congestion. In the spirit of maintaining comprehensiveness, one SSLS circuit was included in this comparison. Figures a and b illustrate the two traditional DSLS circuits that were evaluated in this analysis. The working principle is as follows Assume the input in high. Transistor ML1 switches on and node nL1 is pulled down to gnd. At the same time inverter I1 switches transistor MR1 off and node nR1 is charged till VDD. Since the gate voltages of the transistors ML2 and MR2 are fixed to VDD the transistors ML2 and MR2 are respectively switched Even future SRAM cells may need such converters for ensuring low sub threshold current and stable operation, .For example, the raised voltage necessary for such memory cells must be kept high, independent of device scaling, to ensure data retention characteristics, although the operating voltage for peripheral logic circuits can be scaled down with device scaling.

Consequently, the voltage difference between memory cells and peripheral circuits will grow with device scaling. In addition, interface circuits of chips must operate at quite a high external voltage, although some internal circuits using scaled devices can operate at a not

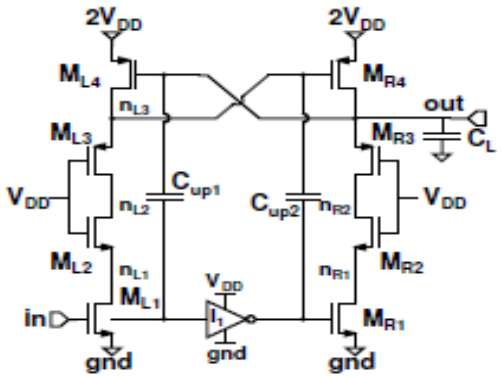

Fig 1.existing system of a standard level shifter

Even some logic gates will have operated at high voltages using raised (boosted) supply voltages and/or negative supply voltages, to manage sub threshold currents. These circumstances unavoidably call for stress voltage-immune circuits for the memory cell and Its related circuits ,interface related circuits and Sub threshold current sensitive circuits .in this paper we discuss the high voltage tolerant circuit Techniques for such circuit with using of conventional level shifter and single supply levels shifter expressed as fraction of the input current. Minimizing the difference is critical path.

III. Proposed System

The proposed LS is a hybrid structure comprising a modified Wilson current mirror and CMOS logic gates. The input and output levels range from a sub-threshold voltage to the standard supply voltage defined in a transistor technology. Bidirectional level conversion is available; that is, input and output levels can be scaled independently

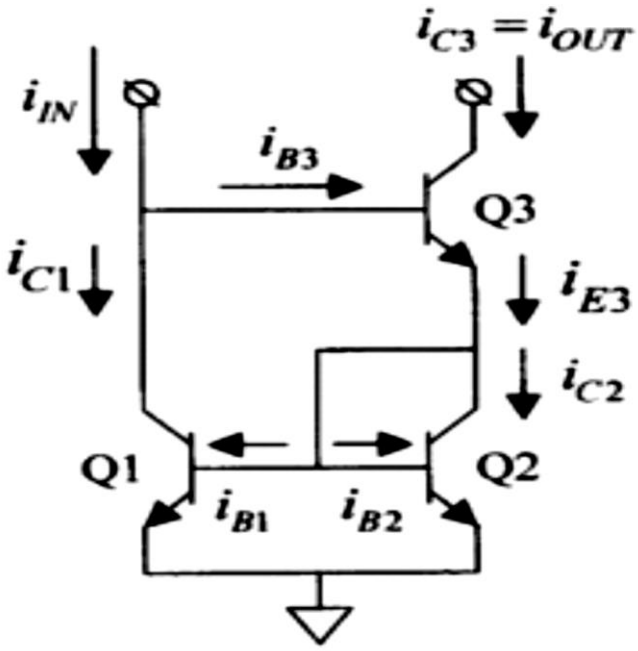

Fig.2 willson current mirror

There are three principal metrics of how well a current mirror will perform as part of a larger circuit. The first measure is the static error, the difference between the input and output currents expressed as a fraction of the input current. Minimizing this difference is critical in such applications of a current mirror as the differential to single-ended output signal conversion in a differential amplifier stage because this difference controls the common mode and power supply rejection ratios. The second measure is the output impedance of the current source or equivalently its inverse, the output conductance. This impedance affects stage gain when a current source is used as an active load and affects common mode gain when the source provides the tail current of a differential pair. The last metric is the pair of minimum voltages from the common terminal, usually a power rail connection, to the input and output terminals that are required for proper operation of the circuit. These voltages affect the headroom to the power supply rails that is available for the circuitry in which the current mirror is embedded.

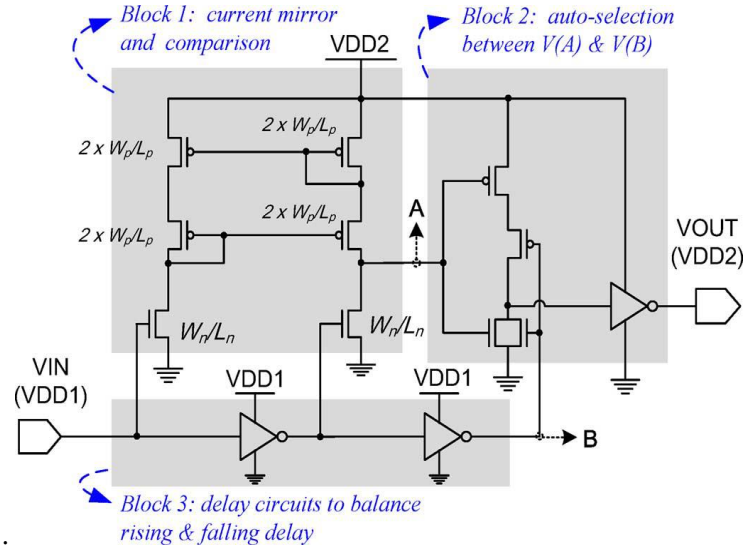

Fig.3 willson current mirror using cmos

This system going to design the novel level shifter based on Wilson current mirror and the buffer based circuit .This level shifter being used in sub-threshold and also the standard supply voltage. This gives the higher performance and the low power consumption based level shifter for portable devices. By using this circuit we are having better performance. The proposed circuit contains the current mirror circuit, buffer circuit and the inverter circuits for the level shifter. For this type of level shifter the standard and the sub-threshold voltages are given to the circuit. The standard supply voltages (VDD2) are given to the current mirror based circuit and the sub-threshold voltages (VDD1) are given to the inverter stages. This will gives the auto selection between the supply voltages and gives the output as standard supply voltage. This will gives the further improvement for the supply voltages based level shifters.

IV. Simulation Results

The existing system of a cross level shifter circuit diagram and a waveform analysis using tanner EDA software

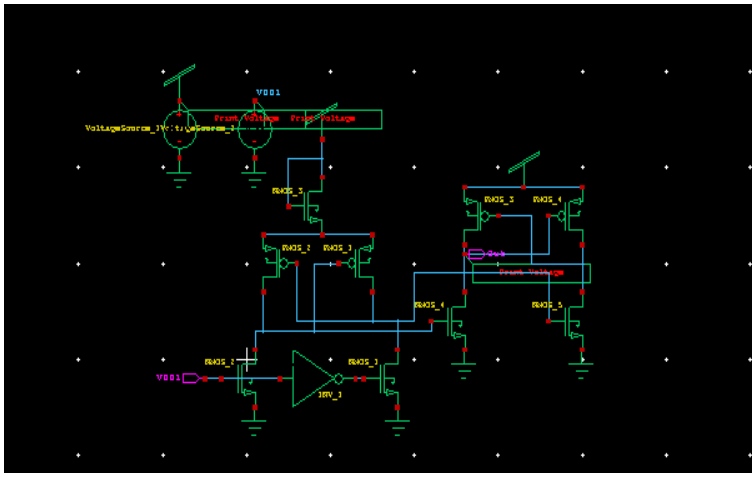

Fig. 4 cross coupled circuit using tanner

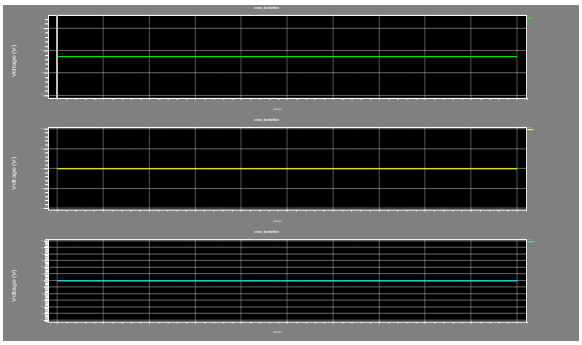

Fig.5 o/p waveform of cross coupled

Existing system of a cross coupled circuit to analyze a input and output.10v is given to the input but 8.5 only obtained the output voltage So willson based current mirror is used .

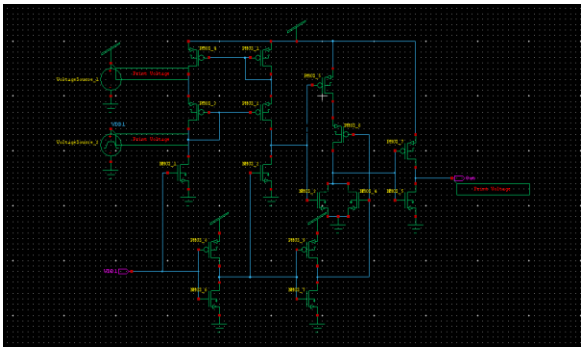

Fig.6 willson current mirror circuit

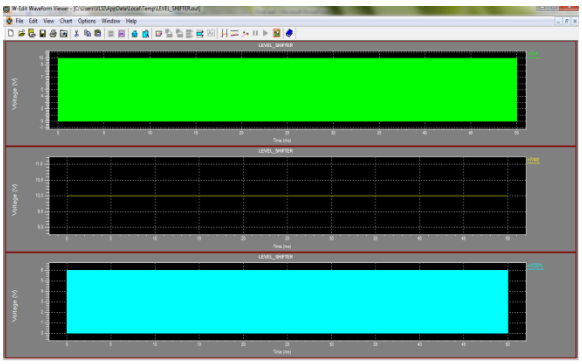

Fig.7 o/p waveform of willson current mirror

The result has been analysed and verified by the existing and proposed circuit of a level shifter. Then the willson current mirror using CMOS circuit input are given to the 10v output also obtained the 10v.so power also reduced.

V. CONCLUSION

Level shifters are usually used to reduce the power. Conventional level shifting methods causes delay variation due to different current driving capabilities of transistors and large power consumption .This proposed method introduces a Wilson current mirror circuit using buffer based circuit. This current mirror circuit will reduce the delay variation and thus provide high performance and low power consumption. The circuit can be used for level shifter in portable devices.

VI. FUTURE WORK

Wilson current mirror circuit consumes only low power and it provides high performance. we have to implement a cascade current mirror circuit using PTL based level shifter .The combination of level shifters will results in reduced power and improved performance compare to the Wilson current mirror circuit. It gives more important to the delay variation

REFERENCES

[1] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 3–29, Jan. 2012.

[2] T.-T. Liu and J. M. Rabaey, "A 0.25 V 460 nW asynchronous neural signal processor with inherent leakage suppression," *IEEE J. Solid- State Circuits*, vol. 48, no. 4, pp. 897–906, Apr. 2013.

[3] Y. Zhang, F. Zhang, Y. Shakhsheer, J. D. Silver, A. Klinefelter, M. Nagaraju, J. Boley, J. Pandey, A. Shrivastava, E. J. Carlson, A. Wood, B. H. Calhoun, and B. P. Otis, "A batteryless 19 WMICS/ISM-band energy harvesting body sensor node SoC for ExG applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 199–213, Jan. 2013.

[4] T. Lin, K.-S. Chong, J. S. Chang, and B.-H. Gwee, "An ultra-low power asynchronous-logic in-situ self-adaptive system for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 573–586, Feb. 2013.

[5] S. Lütkemeier, T. Jungeblut, H. K. O. Berge, S. Aunet, M. Porrmann, and U. Rückert, "A 65 nm 32 b subthreshold processor with 9T multi-Vt SRAM and adaptive supply voltage control," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 8–19, Jan. 2013.

[6] S. Hsu, A. Agarwal, M. Anders, S. Mathew, H. Kaul, F. Sheikh, and R. Krishnamurthy, "A 280 mV-to-1.1 V 256 b reconfigurable SIMD vector permutation engine with 2-dimensional shuffle in 22 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2012, pp. 178–180.

[7] S. Lütkemeier and U. Rückert, "A subthreshold to above-threshold level shifter comprising a wilson current mirror," *IEEE Trans Circuits Syst. II, Exp. Briefs*, vol. 57, no. 9, pp. 721–724, Sept. 2010.

[8] S. N. Wooters, B. H. Calhoun, and T. N. Blalock, "An energy-efficient subthreshold level converter in 130-nm CMOS," *IEEE Trans Circuits Syst. II, Exp. Briefs*, vol. 57, no. 4, pp. 290–294, Apr. 2010.

[9] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," *IEEE J. Solid State Circuits*, vol. 47, no. 7, pp. 1776–1783, July 2012.

[10] M. Lanuzza, P. Corsonello, and S. Perri, "Low-power level shifter for multi-supply voltage designs," *IEEE Trans Circuits Syst. II, Exp. Briefs*, vol. 59, no. 12, pp. 922–926, Dec. 2012.

[11] S. Ali, S. Tanner, and P.-A. Farine, "A robust, low power, high speed voltage level shifter with built-in short circuit current reduction," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Aug. 2011, pp. 142–145.

[12] S.-C. Luo, C.-R. Huang, and L.-Y. Chiou, "Minimum convertible voltage analysis for ratio less and robust sub-threshold level conversion," in *Proc. Int. Symp.Circuits Systems (ISCAS)*,May 2012, pp. 2553–2556.

[13] Y.-S. Lin and D. M. Sylvester, "Single stage static level shifter design for sub-threshold to I/O voltage conversion," in *Proc. Int. Symp. Low Power Electronics Design (ISLPED)*, 2008, pp. 197–200.

[14] I. Chang, J. Kim, K. Kim, and K. Roy, "Robust level converter for subthreshold/ super-threshold operation:100 mV to 2.5 V," *IEEE Trans. VLSI Syst.*, vol. 19, no. 8, pp. 1429–1437, Aug. 2011.

[15] A. Chavan and E.MacDonald, "Ultra low voltage level shifters to interface sub and super threshold reconfigurable logic cells," in *Proc. IEEE Aerospace Conf.*, Mar. 2008, pp. 1–6.