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AN EFFICIENT DOMINO LOGIC DESIGN

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Abstract

The explosive growth in present day technology scenario, now-a-days demand low-power VLSI systems with improved performance. One of the most widely used logics in VLSI design is Domino logic. Domino logic circuits are often used in high performance critical units of microprocessors and also in high speed implementation of high fan in circuits. Domino logic is the technique which overcomes the disadvantage of dynamic logic. The main disadvantage of dynamic logic is that cascading of two different dynamic logics cannot be done. So to avoid that, we go for domino logic. Here the disadvantage of dynamic logic is overcome by simply inserting a static inverter between two stages. So this resembles two dynamic logics connected using a static logic. As technology is scaled down, power supply must be scaled to decrease power consumption which in turn increases leakage current and parasitic capacitance contributing towards increased power dissipation. Here a new domino circuitry is proposed which has very low power dissipation. This is achieved by current comparison based circuitry. The proposed circuitry decreases the parasitic capacitance on the dynamic node, yielding smaller keeper for wide fan-in gates to implement fast and robust circuits. This decreases current contention and leakage current too. The simulation is done using MENTOR GRAPHICS EDA TOOL with 180 nm technology.

Keywords: Domino logic, Leakage-Tolerant, Noise immunity, Wide fan-in, Current Comparison Logic

1. Introduction

The domino logic consists of an ‘n’ type dynamic logic block followed by static Inverter for cascading of dynamic gates. There are two phases of working. They are the Pre-charge phase and Evaluation phase. During Pre-charge phase, the output of the n type dynamic gate is charged up to VDD and the output of the inverter is set to Q. During Evaluation phase, the dynamic gate conditionally discharges and the output of the inverter makes a conditional transition from 0→1. The introduction of static inverter has the additional advantage that fan-out of gate is driven by static inverter with low impedance output which increases noise immunity. Also it reduces the capacitance of dynamic output node. Since each dynamic gate has static inverter, only non-inverting logic can be implemented. This is a major limiting factor. Apart from this disadvantage very high speed can be achieved. But while implementing the wide fan-in logic gates using this dynamic logic technology, there are certain disadvantages like

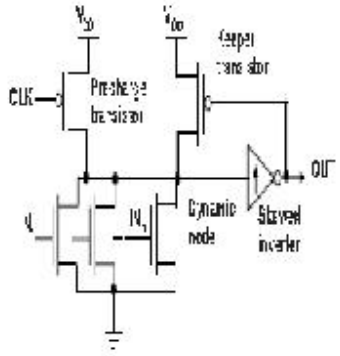
high capacitance on the dynamic node, leakage current due to evaluation phase, high current contention due to upsizing and so on. In order to avoid the above said disadvantages many logics where proposed. But they also had their own demerits. And now new domino logic is proposed which has low leakage without dramatic speed degradation for wide fan-in gates. This technique utilizes the concept of current comparison based domino logic

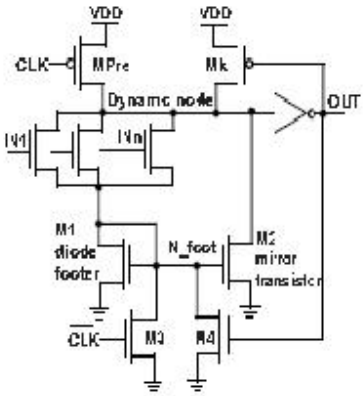
2. Literature Review

There are many existing techniques for this domino logic. Each technique has its own advantages as well as disadvantages. The first technique proposed was the standard footless domino logic technique. J.M. Rabey et al., in 2002 proposed a Standard Footless Domino Logic (SFLD) [1]. This is the most popular dynamic logic and the conventional one. Here a PMOS keeper transistor is used to avoid any unwanted discharge of the dynamic node because of leakage current and charge sharing because of the Pull Down Network (PDN) which happens during the evaluation phase. So the noise robustness is made high. But keeper upsizing increases current contention between the keeper transistor and evaluation network increasing power consumption and evaluation delay of domino circuits. H. Suzuki, C. Kim and K. Roy proposed logic called Diode Partitioned Domino in Feb 2002 [5] for fast tag comparators. It reduces the parasitic capacitance and enables smaller keeper in highfan-in gates. The diode circuit is also improved by an enhanced diode that boosts up the gate voltage of the NMOS diode. Yet it suffers from power dissipation value being little greater. M.H Anis, M.W. Allam and M.I. Elmsary in May 2002 [2] proposed a logic called as High Speed Domino logic (HSD). Reduce the current drawn through the PMOS keeper and the NMOS PDN. This helps in keeping the large PMOS keeper without performance degradation and leakage current. However the area and power overhead of the clock delay circuit will still be there. H. Mahamoodi and K. Roy proposed a logic named as Diode Footed Domino logic (DFD) in March 2004[3]. A diode footer transistor is used in series with the evaluation network. So robustness and noise the replica circuit. For equal noise margin, more legs are possible. Gate is faster with same number of gates. A fairly large safety factor is needed to account for random on- die process variation especially FET Vt variation. Ali Peravi and Mohamed Asyaei proposed a robust low leakage controlled keeper based domino in 2012 [11] which works on reduction of leakage current and power but yet suffers from serious efficiency issues in terms of area and delay. A. Alvandpur, R. Krishnamurthy and K. Sourrty proposed a logic called Conditional Keeper Domino logic in Jan 2007. This consists of small and large keeper transistors. The conditional keeper domino has certain disadvantages such as limitations on increasing the delay and power dissipation due to upsizing. Y. Lih, N. Tzartzanis and W.W Walker proposed a leakage current replica keeper dynamic circuit in Jan 2007. It improves scaling of the dynamic logic gates

3. Proposed Design

The proposed design works in such a way that it contributes towards reduced power dissipation by reducing the capacitance, leakage current and current contention. The problems can be solved by separating the keeper transistor from the PDN which implements the logic function by using a comparison circuit. This circuit compares the worst case leakage current. Normally in domino logic, in the Pull Up Network (PUN) only one pMOS transistor is used instead of ‘n’ transistors where ‘n’ corresponds to the fan-in. the main logic will be implemented with the PDN. By reducing the number of transistors capacitance decreases. Few transistors means limited switching. (Charging and discharging) of the capacitor. Thus dynamic power consumption gets reduced because the main source of dynamic power consumption is capacitance switching. Leakage current occurs due to unnecessary flow of current between the drain and the source of the transistor. This leakage current can be avoided by the “stacking effect”. Stacking effect says that when two or more transistors in series are at off condition, the leakage current can be reduced. A keeper transistor is used so that this transistor supplies a small current from the supply to the dynamic node.





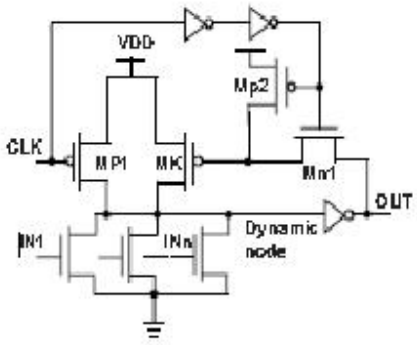


Figure 1: SFLD **Figure 2: DFD** **Figure 3: HSD**

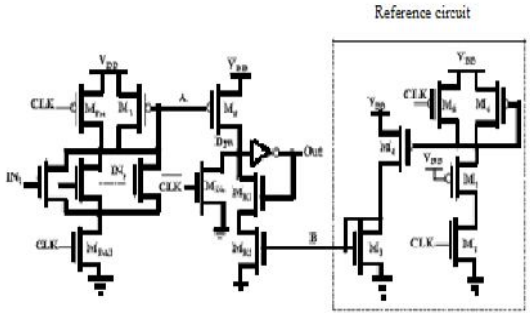


Figure 4: Proposed Domino or gate

Therefore charge stored is preserved for the needed conditions. Current contention is also a serious problem. By disabling the keeper for particular amount of time temporarily during the dynamic gate switching, the current contention problem is avoided. The proposed wide fan-in domino gate OR gate is shown in Figure 4. In the proposed circuit current of the PUN is reflected by transistor M2 and also compared with reference current, which replicates the leakage current of the PUN. The proposed circuit is implemented with nMOS circuit to implement the logic function. eg: OR gate. The source and body terminals of the pMOS transistor are connected together so that the body effect is eliminated. The transistor M1 is in diode configuration which means the drain and the gate are connected together. This helps in decreasing the leakage current reduction by using the stacking concept. Addition of M1 results in leakage reduction of evaluation network by stacking effect. The stacking effect decreases the drain source voltage of evaluation transistors and hence decreases the Drain Induced Barrier Lowering (DIBL). The DIBL is caused due to threshold fluctuation which in turn is caused due to high current flow between the drain and the source. So by decreasing power Vds, DIBL is reduced. In the circuit shown in the Fig a, transistor M5 plays an important role in reducing standby power dissipation. The reference circuit shown in the figure generates the reference current. So by incorporating the above said methodologies effective power dissipation reduction is achieved. There are two phases of working. In the first phase called as Pre-Charge phase the clock input to the given circuit is logic low state (‘0’). The keeper transistors are ‘ON’ in this condition. In the second phase called the Evaluation phase, clock input is at logic high state (‘1’). Also there occur two different conditions in this phase. The first condition is when all the inputs are at logic ‘0’.The second condition is when at least one input is at logic ‘1’.

The keeper transistors are ON/OFF depending upon the input. In the second condition since at least one input is high, path exists to the ground because in the PDN nMOS transistors are used also during this state M1 transistor is in ON condition. So current in the PUN is high. This is reflected by the transistor M2. This causes the keeper transistors to turn off. This ultimately reduces the current contention problem.

4. Simulation Results

The proposed circuit is compared with the existing SFLD, DFD and HSD in terms of power and area for wide fan-in of 4. The simulation is done using MENTOR GRAPHICS EDA tool with 180 nm technology. From the TABLE 1, the power dissipation of proposed circuit is found to be lesser than all the existing works. But the area increases for the proposed logic than the previous techniques. The comparison is done for 4 input wide fan-in OR gate. The reason to choose the wide fan-in gate is that it has many leaky paths and due to this power dissipation increases heavily. So by incorporating the proposed domino logic in wide fan-in gates power dissipation has found to be decreased. From TABLE 2 it is visible that the SFLD logic has the highest power dissipation but very less area overhead but the proposed domino logic has very low power dissipation with very high area overhead while comparing with existing techniques like HSD and DFD logic. From TABLE 3, it is clear that the output noise voltage of the proposed domino logic has reduced visibly while comparing with the input noise voltage. As seen from TABLE 4, the measured parameters are normalized with respect to SFLD logic and the performance comparison is made between the proposed logic and the existing SFLD logic.

Table 1: Power dissipation and Area comparison between 4 input SFLD and Proposed Domino logic

LOGIC	POWER DISSIPATION	AREA
SFLD	818.34µW	168 µm
PROPOSED LOGIC	1.667 µW	456 µm

Table 2: Power dissipation and Area comparison between different Domino logics

LOGIC	POWER DISSIPATION	AREA
SFLD	818.34 µW	168 µm
HSD	274.37 µW	228 µm
DFD	299.60 µW	252 µm
PROPOSED LOGIC	1.6877 µW	456 µm

Table 3: Input and Output noise voltage of proposed Domino logic

LOGIC	INPUT NOISE VOLTAGE	OUTPUT NOISE VOLTAGE
4 INPUT	40.02V	39.54V
8 INPUT	37.29V	35.94V
16 INPUT	41.62V	40.64V

Here Figure Of Merit is calculated. Figure Of Merit (FOM) is the quantity that is used to characterize the performance of a device or system or method, relative to its alternatives. Unity Noise Gain (UNG) is also calculated. Unity Noise Gain (UNG) is the input noise amplitude that causes the same noise voltage to be caused at the output. The formula for the FOM is

$$FOM = (UNG\ \ norm)/(P_{tot-norm} * t^2_{p-norm} * \sigma_{Delay-norm} * A_{norm})$$

From the TABLE 4, the FOM for the proposed domino logic is higher than the existing SFLD domino logic. From the FIGURE 5 it is inferred that the power dissipation and delay are lesser for the proposed logic than the SFLD logic whereas the FOM and area overhead are higher than the SFLD logic.

5. Application: MULTIPLEXER BASED ON PROPOSED DOMINO LOGIC

A new multiplexer is proposed based on the proposed domino logic. The Figure 5 shows the proposed multiplexer. The proposed multiplexer is compared with the existing Diode Footed Domino multiplexer. Mostly multiplexers are used in register files of the processor memory. So it is very important that power dissipation for the multiplexers should be very less. The proposed multiplexer shown in the figure is a 4:1 multiplexer. S0 to Sn are the select lines and D0 to Dn are the data input lines. The Table 5 shows the performance comparison between the proposed multiplexer and already existing DFD multiplexer. From the TABLE 5 it is seen that the proposed multiplexer has low power dissipation on comparison with the DFD multiplexer but the delay and area are higher.

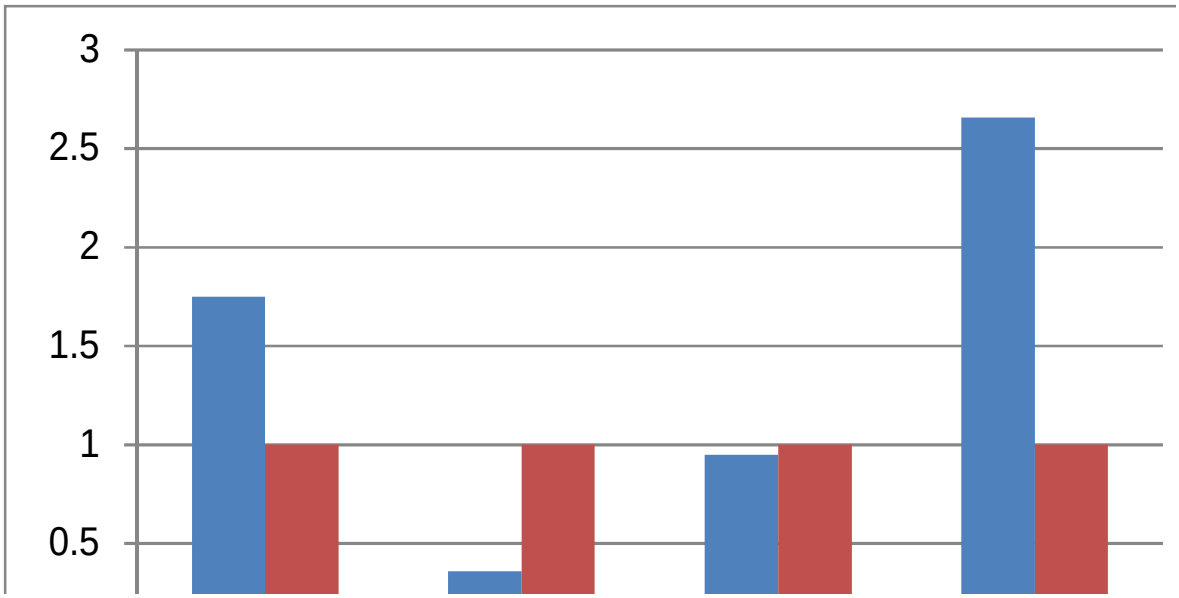


Figure 5: Performance comparison chart between SFLD and Proposed Domino logic

Table 4: Performance comparison between SFLD and proposed Domino logic

MEASURED PARAMETERS	SFLD n = 4	SFLD n = 8	SFLD n = 16	PROPOSED LOGIC n = 4	PROPOSED LOGIC n = 8	PROPOSED LOGIC n =16
UNG	1	1	1	1.04	1.12	1.12
NORMALISED POWER	1	1	1	0.96	0.98	0.95
NORMALISED AREA	1	1	1	2.96	2.2	1.75
NORMALISED DELAY	1	1	1	0.36	0.36	0.36
NORMALISED √DELAY	1	1	1	0.77	0.79	0.77
FOM	1	1	1	1.32	1.86	2.66

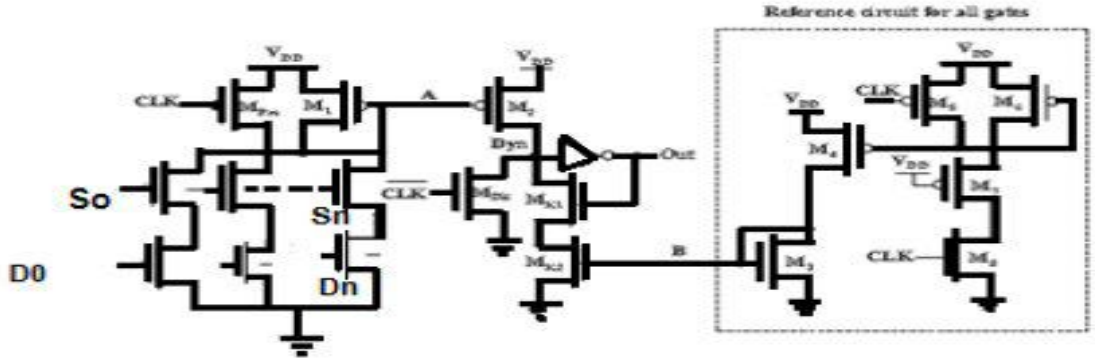


Figure 6: Multiplexer based on proposed Domino logic

6. Conclusion

The domino logic circuitry suffered mainly due to increased power dissipation because of leakage current in the evaluation network and also due to current contention because of keeper upsizing as a result of technology scaling. In order to avoid such problems the new domino logic is proposed based on the current comparison concept. Here the main idea is to compare the evaluation current of gate with the leakage current. The proposed domino logic has power dissipation of about 1.667 µW, 842.50 µW and 880.17 µW for wide fan-in of 4,8 and 16 which is very less compared to SFLD logic which has power dissipation of about 818.342 µW,851.50 µW and 922.53 µW for the same number of fan-ins. Delay is also found to be lesser for the proposed domino logic than the existing SFLD logic. But the area for the proposed domino logic is far higher than the SFLD logic. The area for four input OR gate is about 456 µm whereas the existing SFLD logic has very low area of about 168 µm. so area overhead is higher for the proposed domino logic. On comparing the input and output noise voltages of the proposed domino logic, the output noise voltages are 39.54v,35.94v and 40.64 v for wide fan-in of 4, 8 and 16 and the input noise voltages are 40.02v, 37.29v and 41.62 v for the same number of wide fan-in. So it is clear that the output noise has reduced considerably. Also a multiplexer is also designed using the proposed domino logic. On comparison with the existing DFD multiplexer the proposed multiplexer has very low power dissipation of about 11.64 µW whereas the DFD multiplexer has a power dissipation of about 55.06 µW. The delay and area of the proposed multiplexer are 13.328 ns and 910 µm which are higher values than the existing DFD logic's delay and area of about 9.928 ns and 736 µm. So it is visible that the proposed domino logic is efficient in terms of power dissipation, noise robustness and delay with slightly higher area overhead.

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